Living in the White Space: Where SI/PI/EMI Lurk

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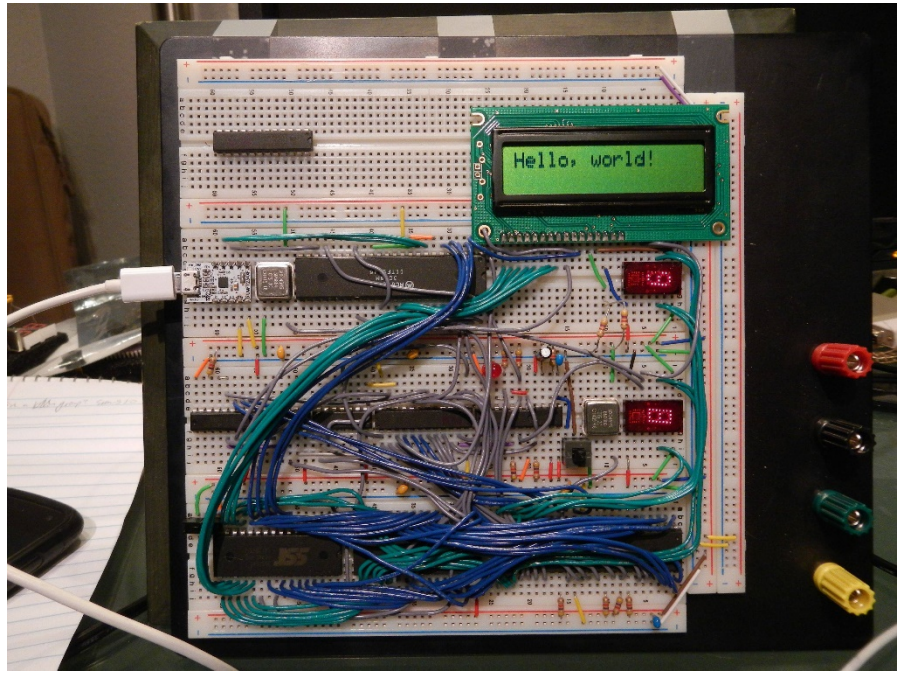
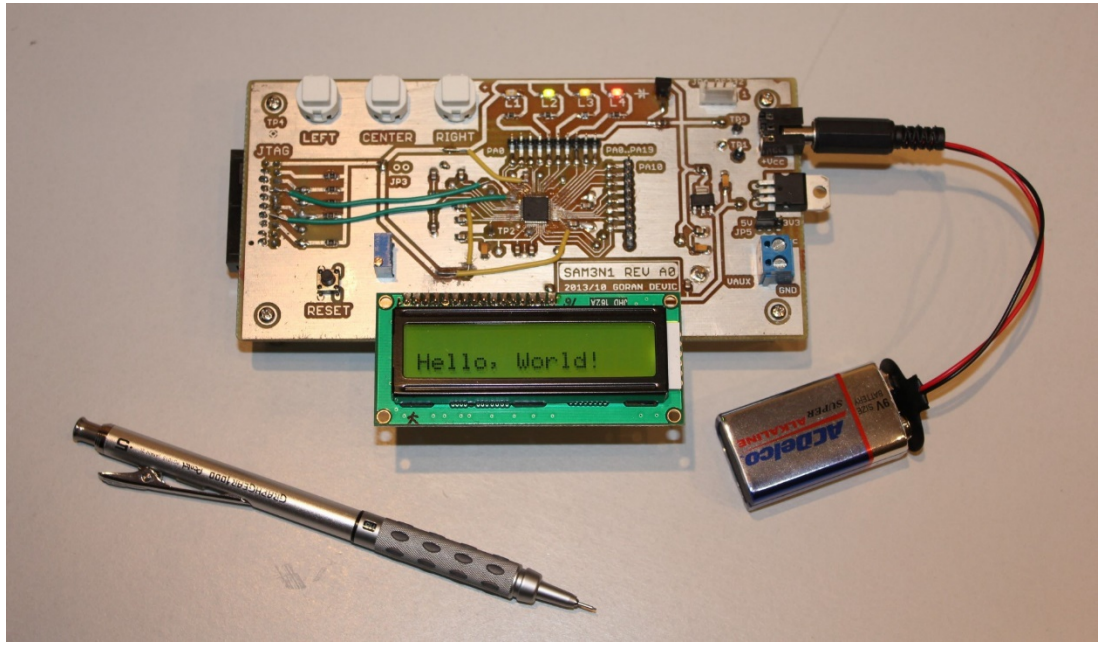
Outline: Some Perspective

- When not to worry
- When to worry, what to worry about, how to sleep better at night
- Seven ***Best Design Practices*** of highly successful designers to reduce:
  - Reflection noise
  - Cross talk noise
  - Ground bounce noise
  - High speed serial links noise
  - Power distribution noise
  - EMI noise
- Best Design Practice means: do this unless you have a strong compelling reason otherwise
- Going forward

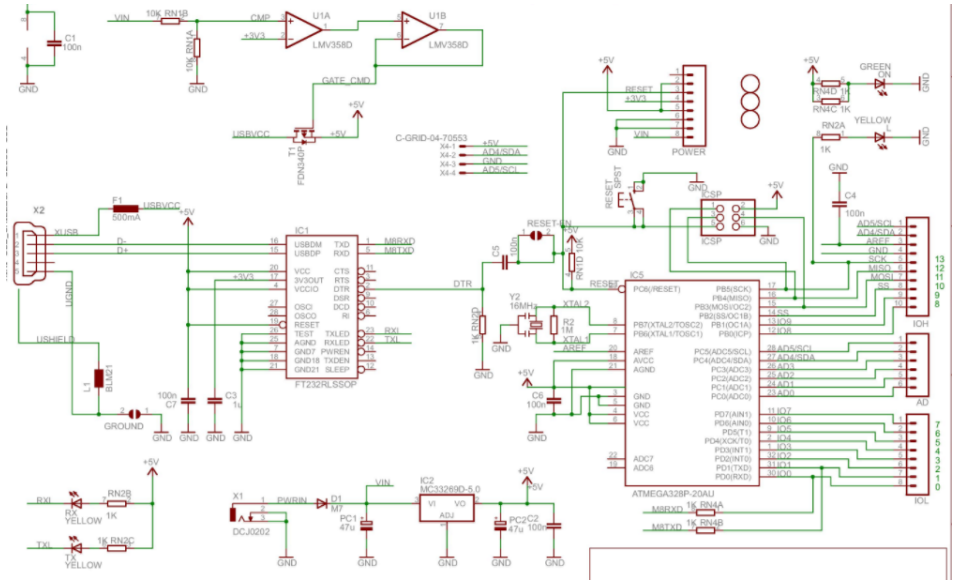
If a Solderless Breadboard Version of the Design Works, So Will the Circuit Board (no matter how it is designed)





If interconnects are transparent
We design for “connectivity”

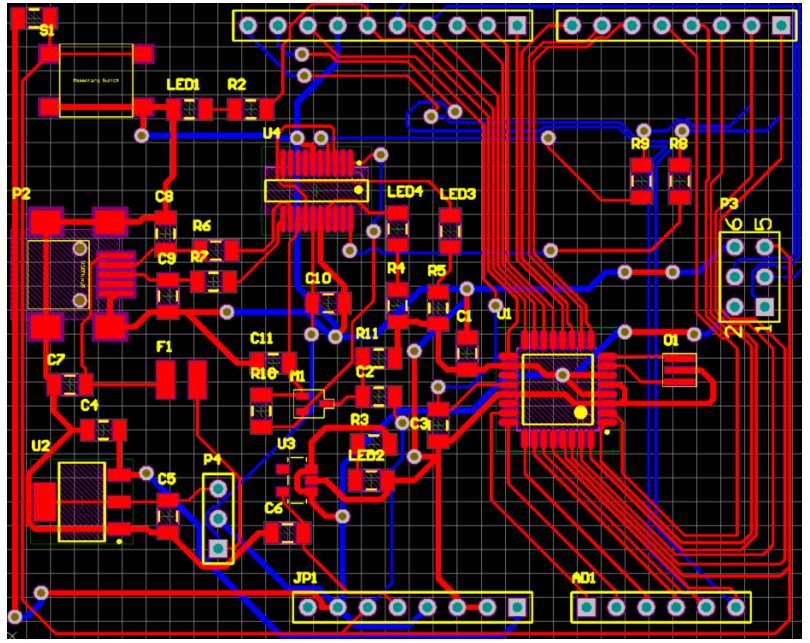
Schematic and Layout Design Information is Not Enough



A schematic says nothing about the interconnects:

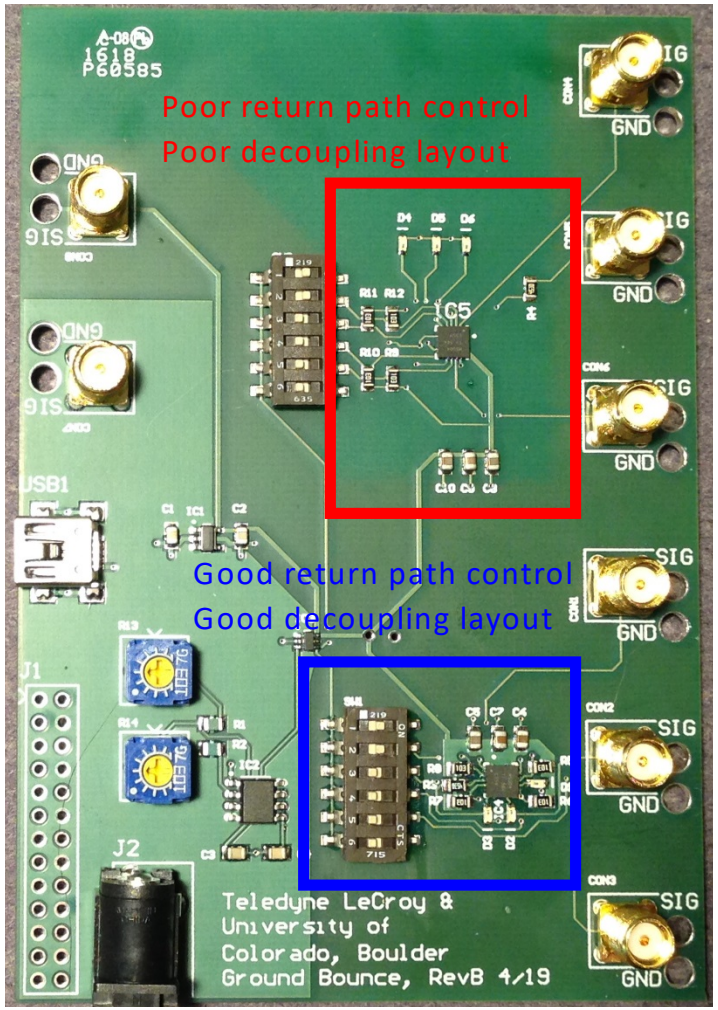
- It's about the BOM
- It's about the Functionality
- It's about the Connectivity
- Wires are transparent- no R, no C, no L, no delay

The layout is the physical design of the interconnects. The *connectivity* matches the schematic.

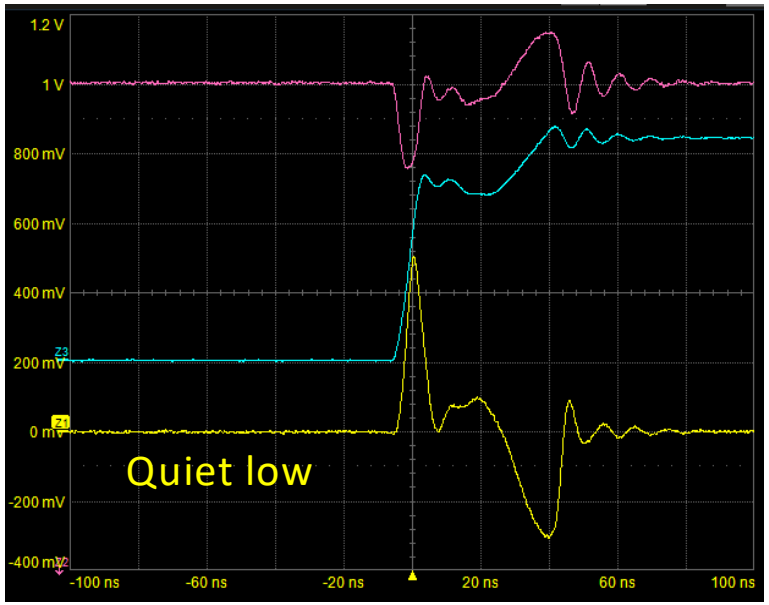


How the layout is implemented may dramatically affect the noise generated: signal integrity, power integrity, EMI

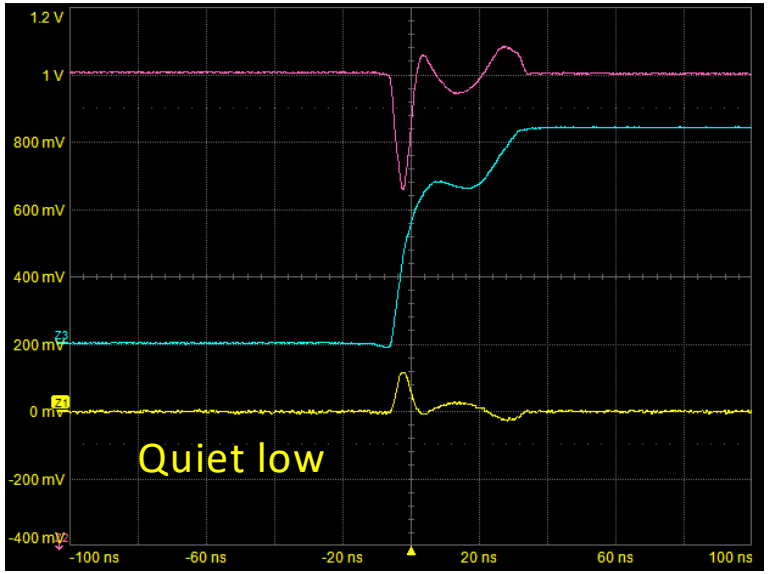
A Simple Example: Screwed Up Return Path, vs Continuous Return Path



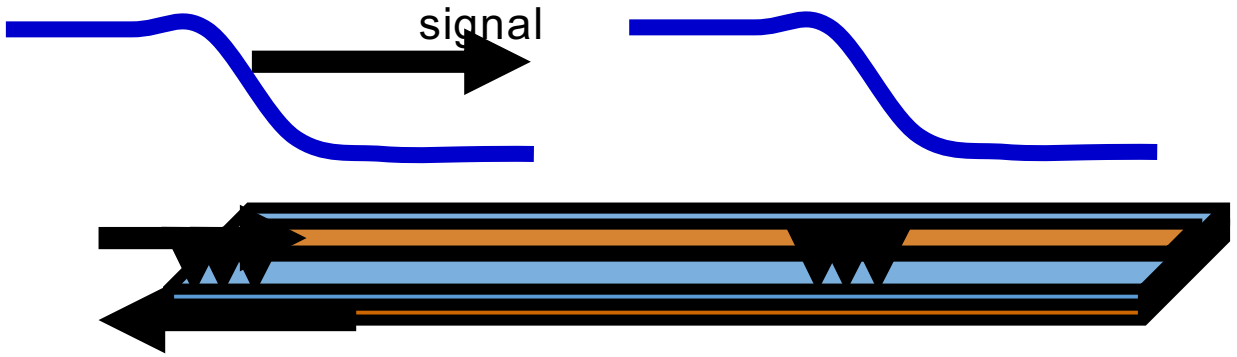
Exactly the same schematic
Only difference is the layout

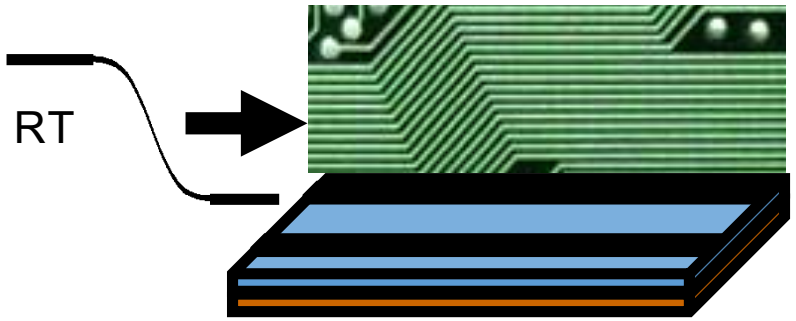


Measured cross talk on a quiet line, not switching



If connectivity is correct, everything else is about controlling noise



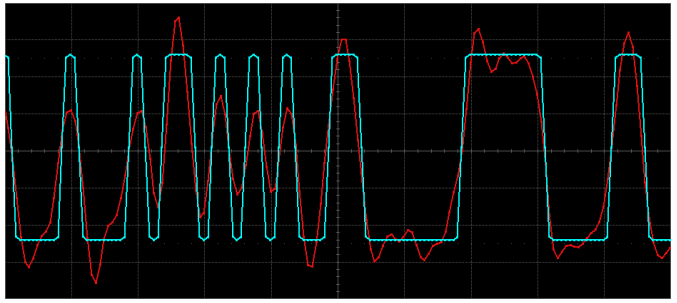


	Self aggression noise	Mutual aggression noise
Signals and uniform returns	Reflections, losses, routing topology, terminations, driver impedance, discontinuities	Cross talk in uniform transmission lines, Near end cross talk far end cross talk
Signals and shared, distorted returns	Reflections from discontinuities, bandwidth limitations	Ground bounce in shared, return path discontinuities (common impedance of the return path)
Power distribution elements	VRM noise, IC dI/dt noise	From PDN onto the ICs
To external world		Radiated emissions ***to*** external world Susceptibility ***from*** external world

SI, PI and EMI problems live in the wires and the white space of the schematic

- *The schematic says nothing about noise*
- *The layout says nothing about noise*
- *Noise arises from the combination of:*

Input signals + Maxwell's Equations + Boundary conditions = Output signals

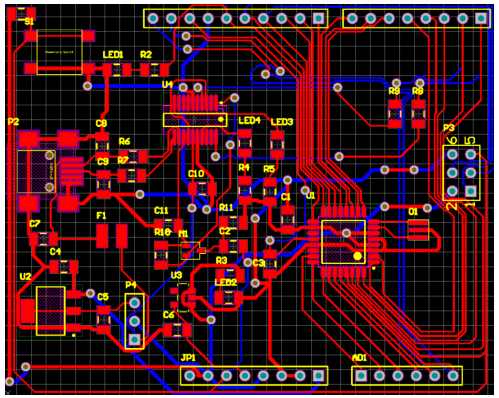


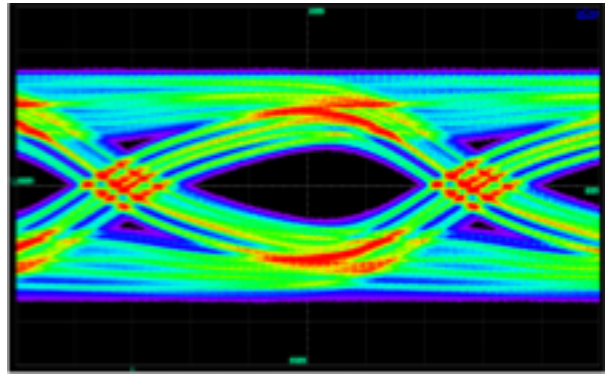
$$\Psi = \oiint_S \mathbf{D}\cdot d\mathbf{S} = \iiint_V \rho_v\, dV \quad (\nabla\cdot\mathbf{D}=\rho)$$

$$\oint_C \mathbf{E}\cdot d\mathbf{l} = -\frac{d}{dt}\iint_S \mathbf{B}\cdot d\mathbf{S} \quad \left(\nabla\times\mathbf{E} = -\frac{\partial\mathbf{B}}{\partial t}\right)$$

$$\oiint_S \mathbf{B}\cdot d\mathbf{S} = 0 \quad (\nabla\cdot\mathbf{B}=0)$$

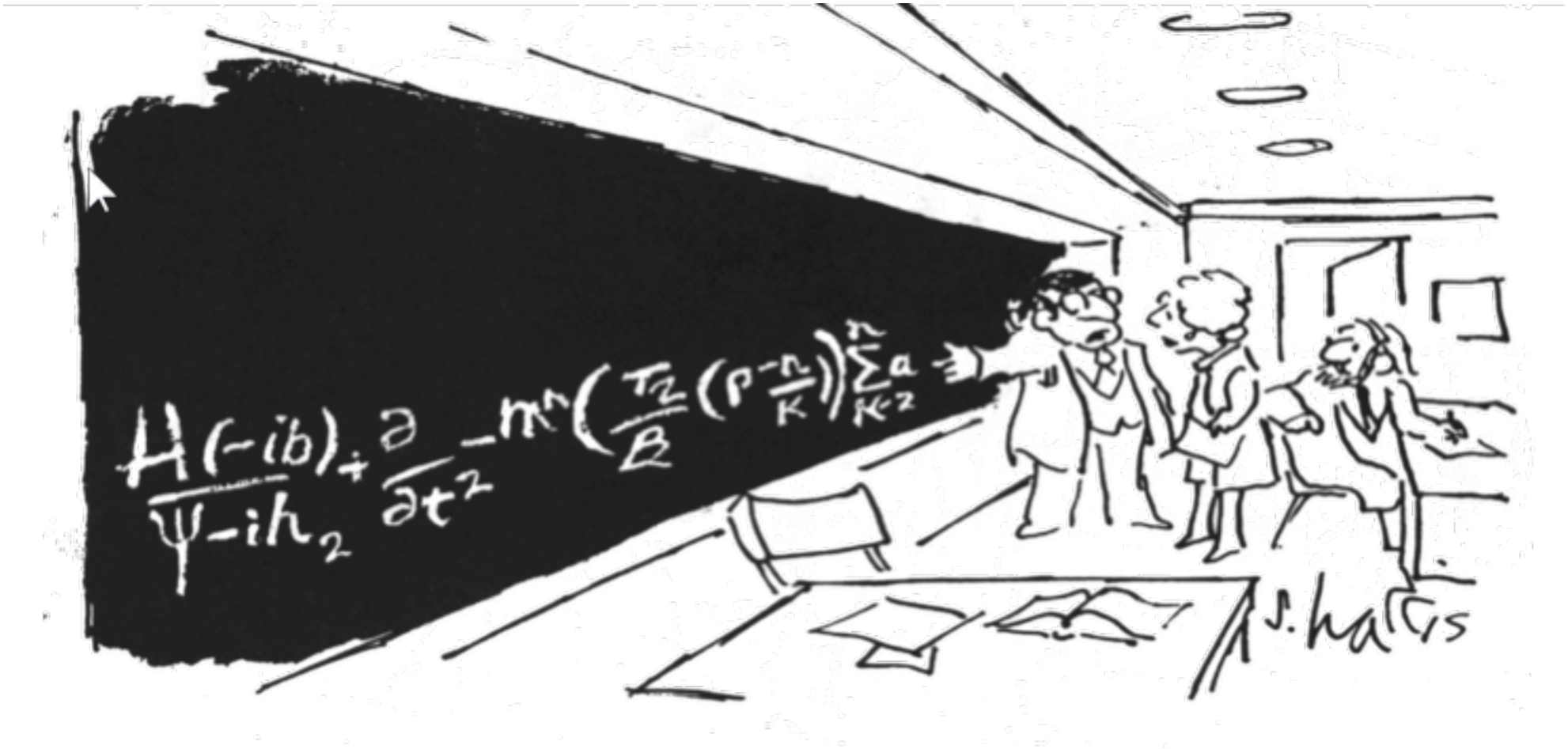
$$\frac{1}{\mu_0\varepsilon_0}\oint_C \mathbf{B}\cdot d\mathbf{l} = \frac{1}{\varepsilon_0}\iint_S \mathbf{J}\cdot d\mathbf{S} + \frac{d}{dt}\iint_S \mathbf{E}\cdot d\mathbf{S}$$



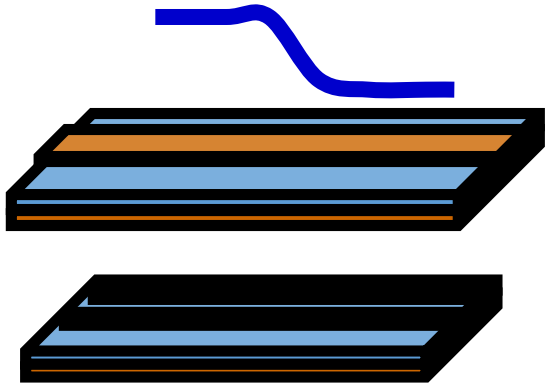


SI, PI and EMI problems live in the wires and the white space of the schematic

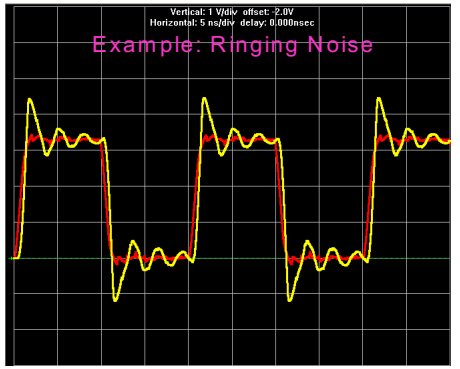
"But this ***is*** the simplified version for the general public"- Sidney Harris



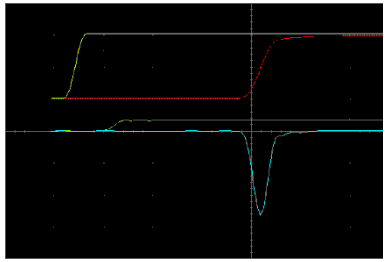
The Six Families of SI/PI/EMC Noise Problems



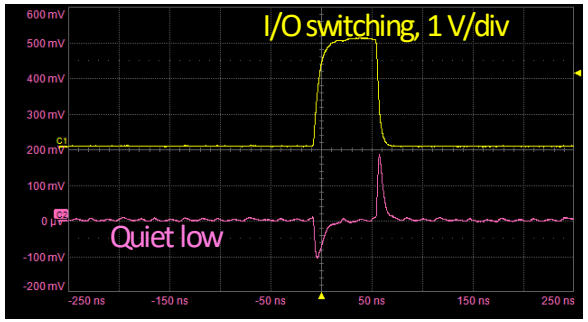
1. Reflection noise



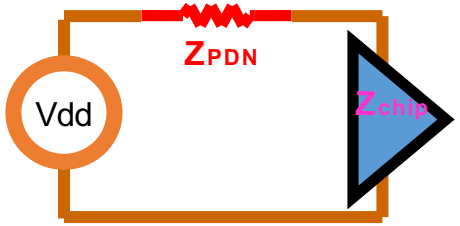
2. Cross talk



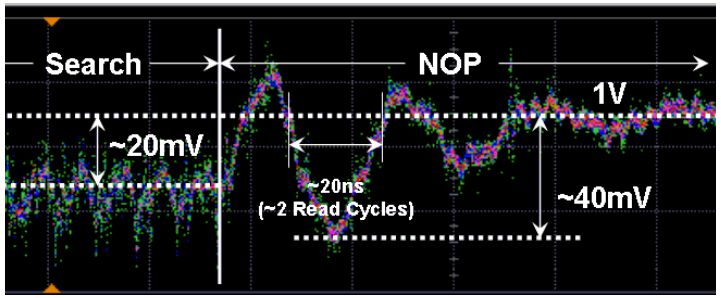
3. Ground (and power) bounce

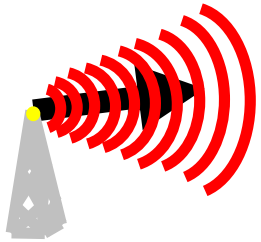


4. Losses (@ Gbps)



5. Rail collapse, voltage droop, power supply noise





6. EMI

Principle #1:
Fastest Way to Solve a Problem is to Identify its Root Cause

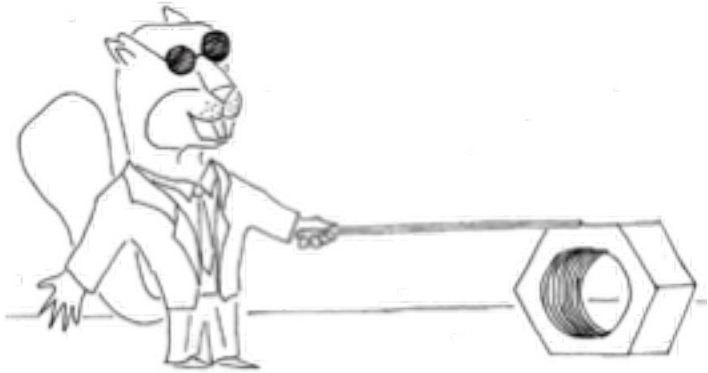
ARE YOU SURE ABOUT THIS, STAN? IT SEEMS ODD THAT A POINTY HEAD AND LONG BEAK IS WHAT MAKES THEM FLY.

16066

(forensic analysis)

If you have the wrong root cause, you will only fix the problem by luck

(even a blind squirrel sometimes finds a nut)



https://howdareyoudesign.wordpress.com/

Turn a Root Cause into a Design Guideline with the Youngman Principle

- Henny Youngman (1906-1998) “King of the one-liners”

  “Take my wife - please!”

  “The food on the plane was fit for a King, Here King, here boy.”

  “A doctor gave a man six months to live. The man couldn't pay his bill, so he gave him another six months.”

  “The Doctor says, "You'll live to be 60!" "I AM 60!" "See, what did I tell you?" ”

  “A man goes to a psychiatrist. The doctor says, "You're crazy" The man says, "I want a second opinion!" "Okay, you're ugly too!" ”

A man goes to a doctor and says, “Doctor, my arm hurts when I raise it. What should I do?”

The doctor says, “Don’t raise your arm.”

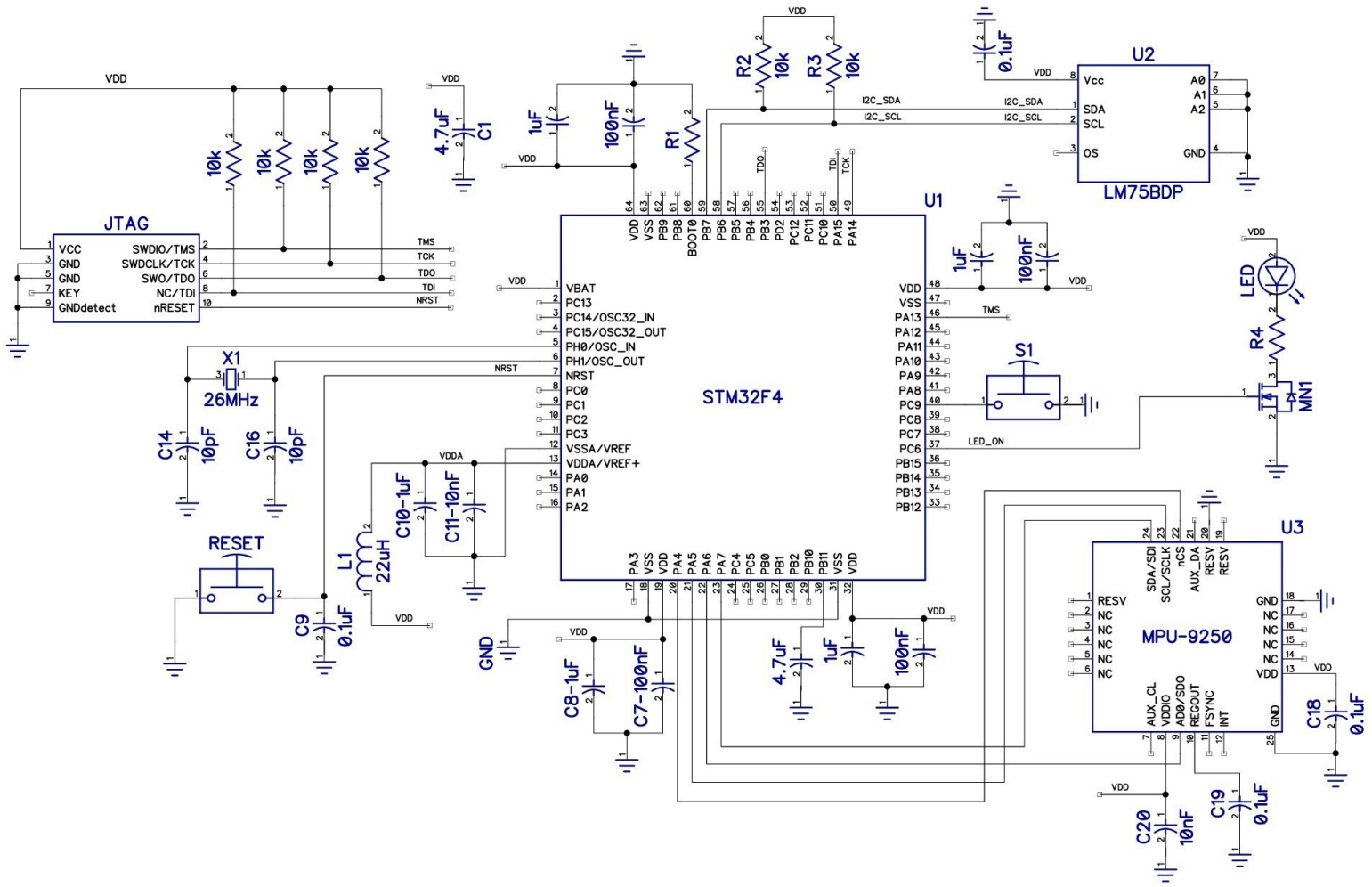
The Design Principle:

“If problem A happens because your design has feature B,

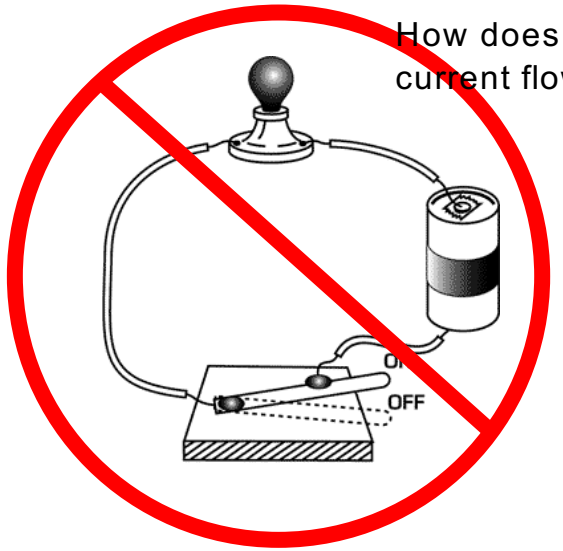
then eliminate feature B from your design”

Signals, return paths, inductance and ground bounce

How does current flow in a circuit? A schematic says NOTHING about how currents flow- just about connectivity



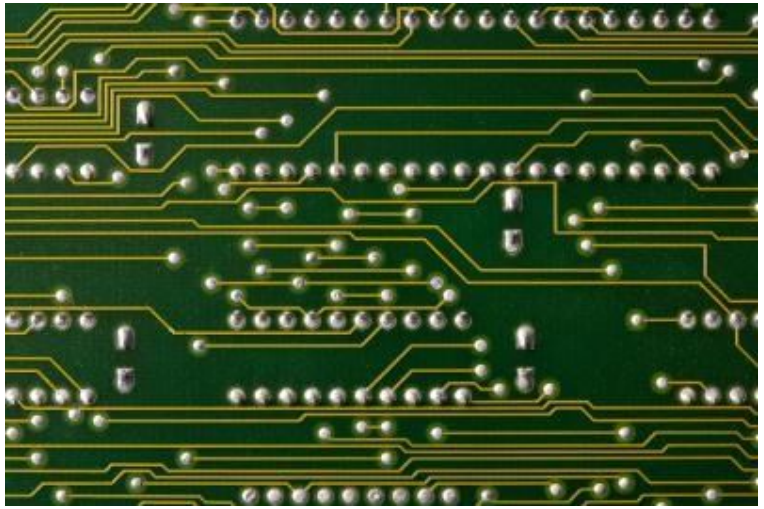
What we learn in 1st grade about current flow is all wrong

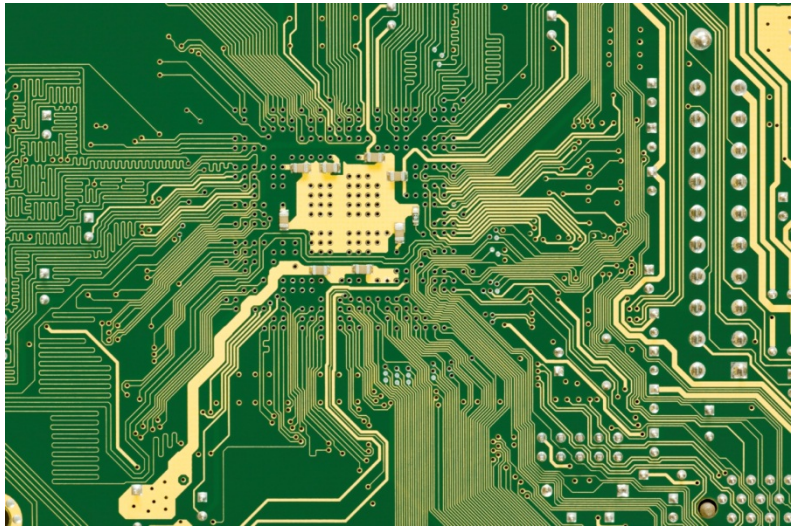


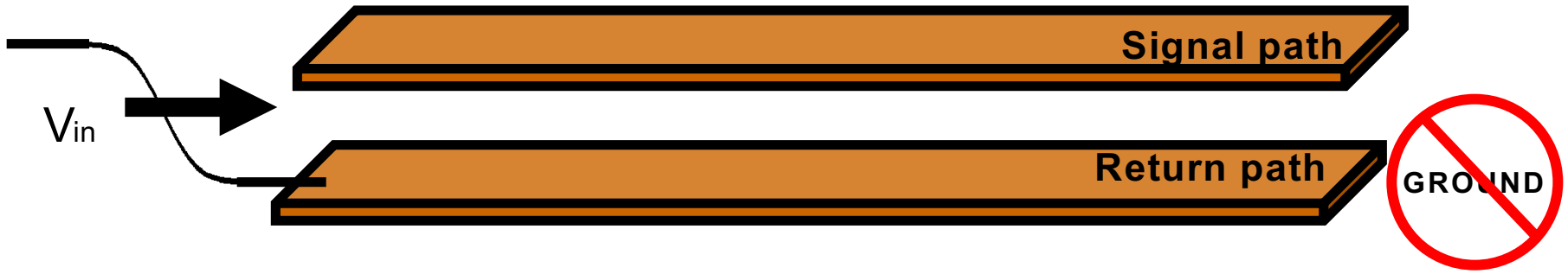
Secrets to Understanding Current Flow

- Don’t confuse DC, steady state, “low frequency” current flow with transient current flow
- Principle #1: Every signal trace has an adjacent return path (nearest conductor)
- Principle #2: Every signal is dynamic- it propagates
- Principle #4: Return current is just as important as the signal current

Essential Principle:
All Interconnects are Transmission Lines

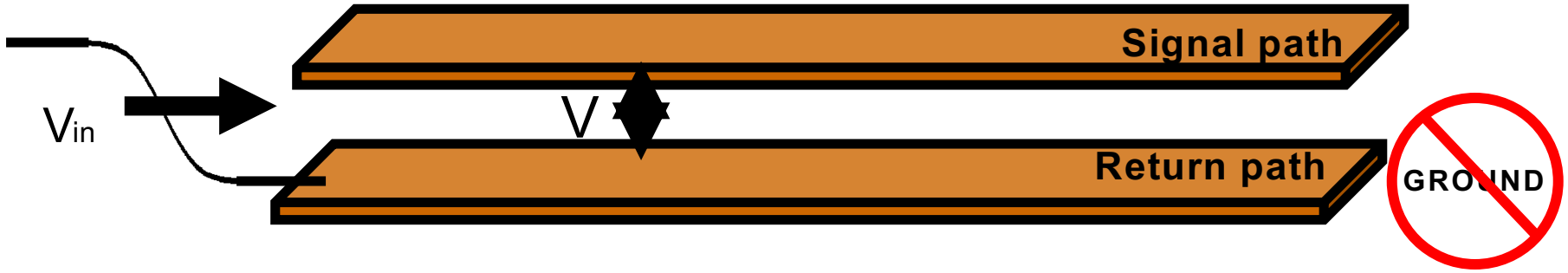




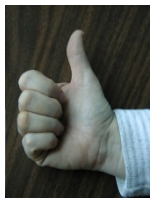


Essential Principle: Signals are Dynamic

All interconnects are transmission lines
A signal as a voltage difference
Signals propagate



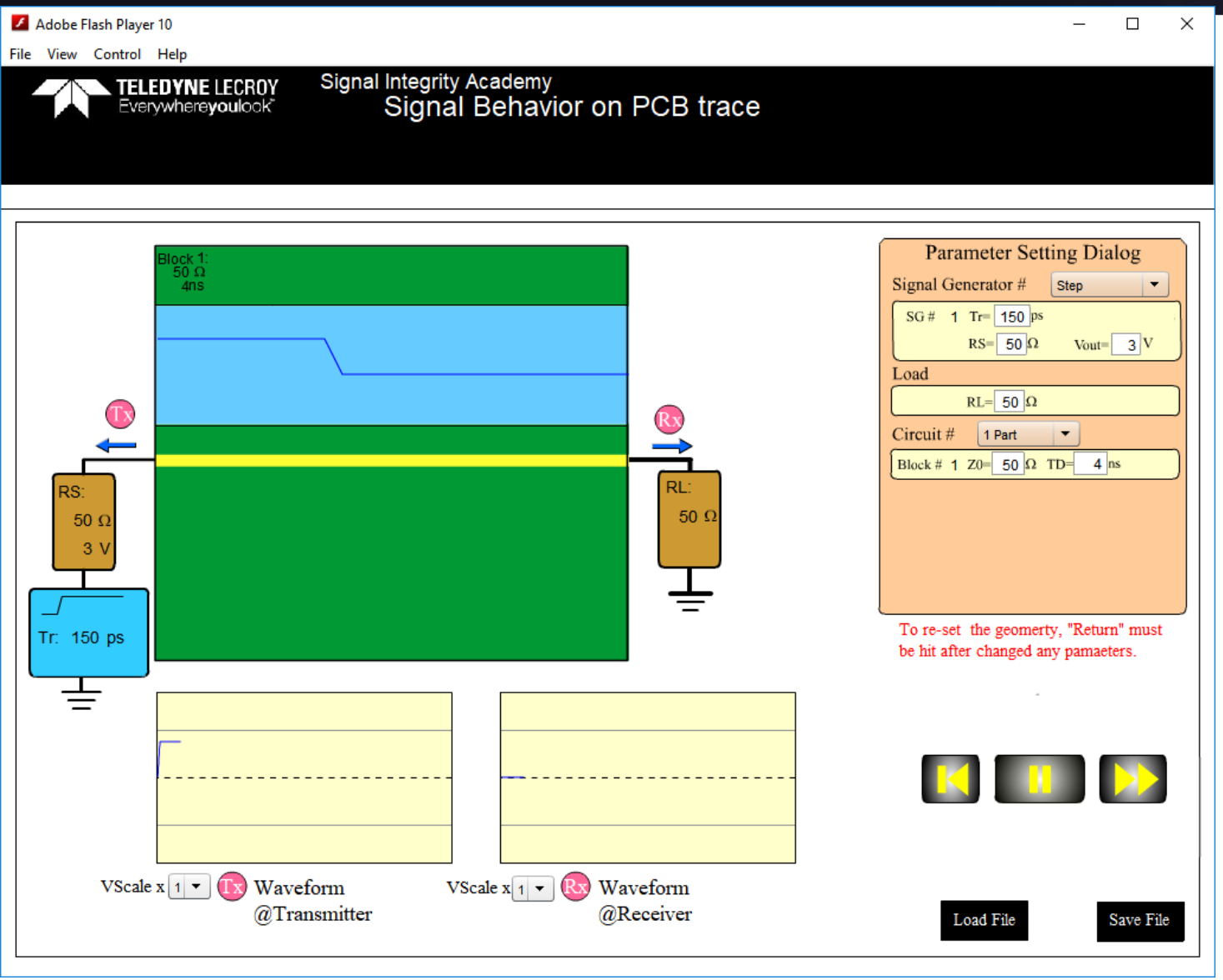
$$v = \frac{12 \frac{\text{inches}}{\text{nsec}}}{\sqrt{Dk}} \quad \text{In FR4 traces} \quad = \frac{12 \frac{\text{inches}}{\text{nsec}}}{\sqrt{4}} = \frac{12 \frac{\text{inches}}{\text{nsec}}}{2} = 6 \frac{\text{inches}}{\text{nsec}}$$



In Coax cable $= \frac{12 \frac{\text{inches}}{\text{nsec}}}{\sqrt{2.2}} = \frac{12 \frac{\text{inches}}{\text{nsec}}}{1.5} = 8 \frac{\text{inches}}{\text{nsec}}$

TD for 1 foot coax = 1.5 nsec, 3 feet in 4.5 nsec ~ 5 nsec

Dynamic Simulation of Propagating and Reflected Signals



Download this free animation tool from

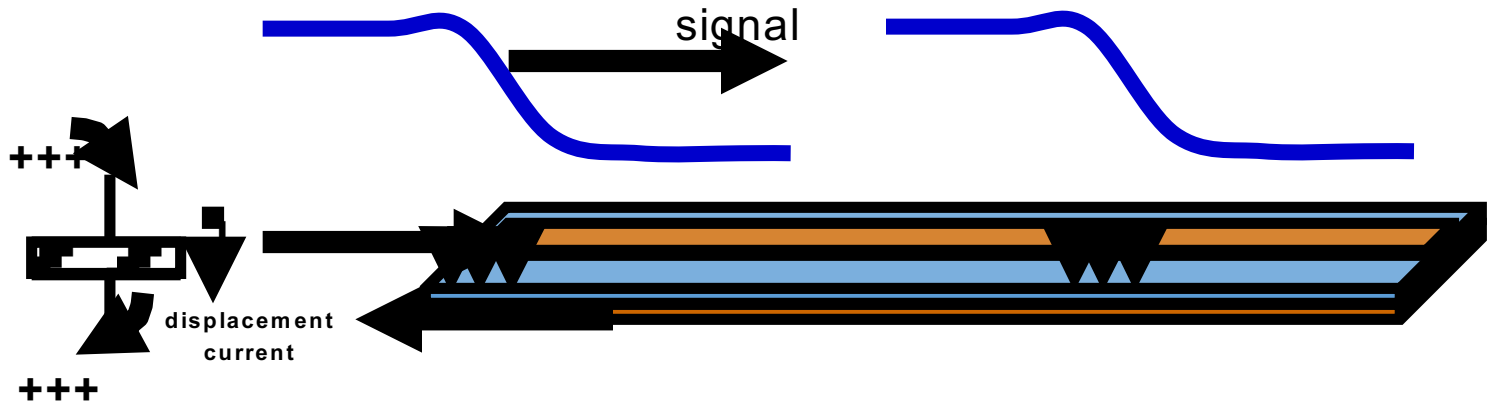
[VRPW-30-16: Yoshi's Animations of Reflections]

But if rise time = 3 nsec, edge extends 3 nsec x 6 in/nsec = 18 inches.

Trace is only 2 inches long- so entire line rises up the same time

Looks like signal goes down line, back the other line

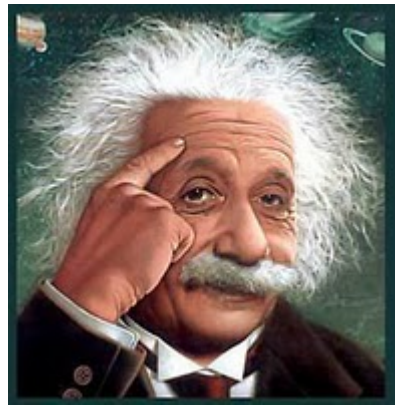
Essential Principle: The Return Current is Just as Important as the Signal Current



The current loop has two directions associated with it:

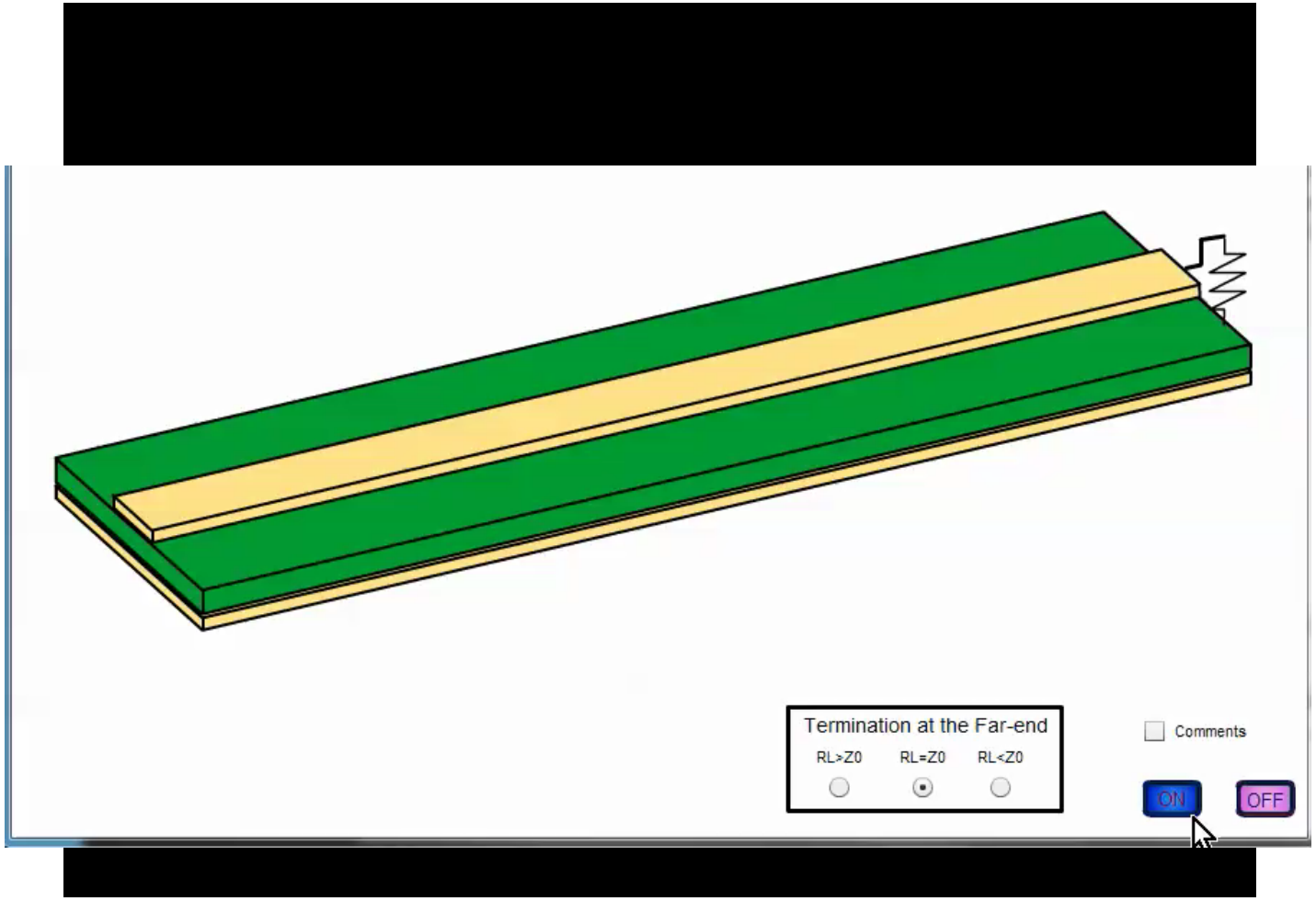
1. ***A direction of propagation***
2. ***A direction of circulation***

They are independent!



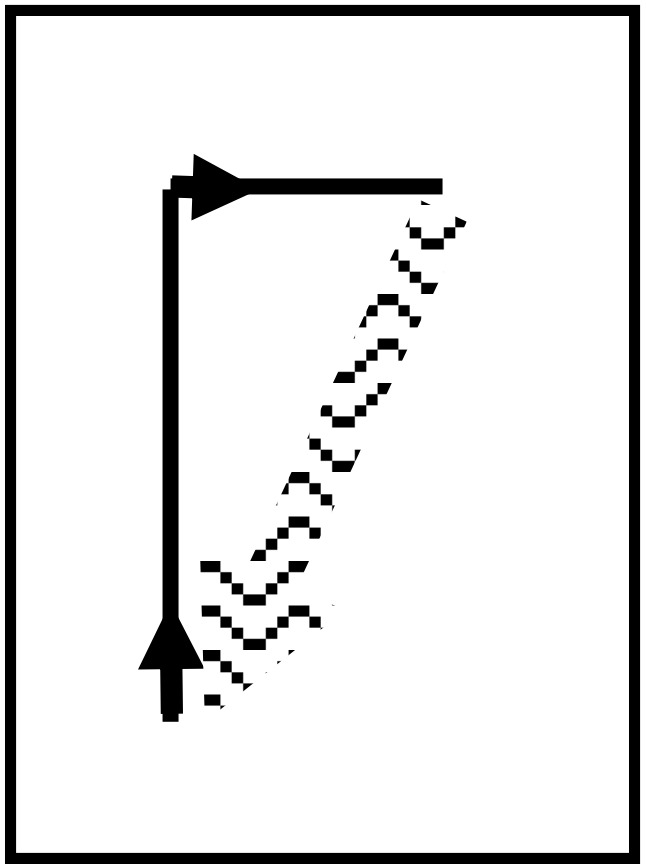
A Way of Thinking About Signal-Return Currents in an Interconnect

Download this flash animation from bethesignal.com



Where Does Return Current Flow?

DC



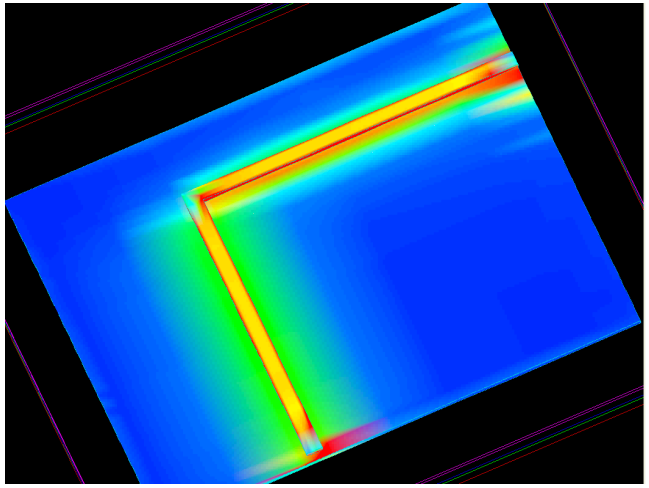
Current takes the path of lowest impedance

$$Z = R + i\omega L$$

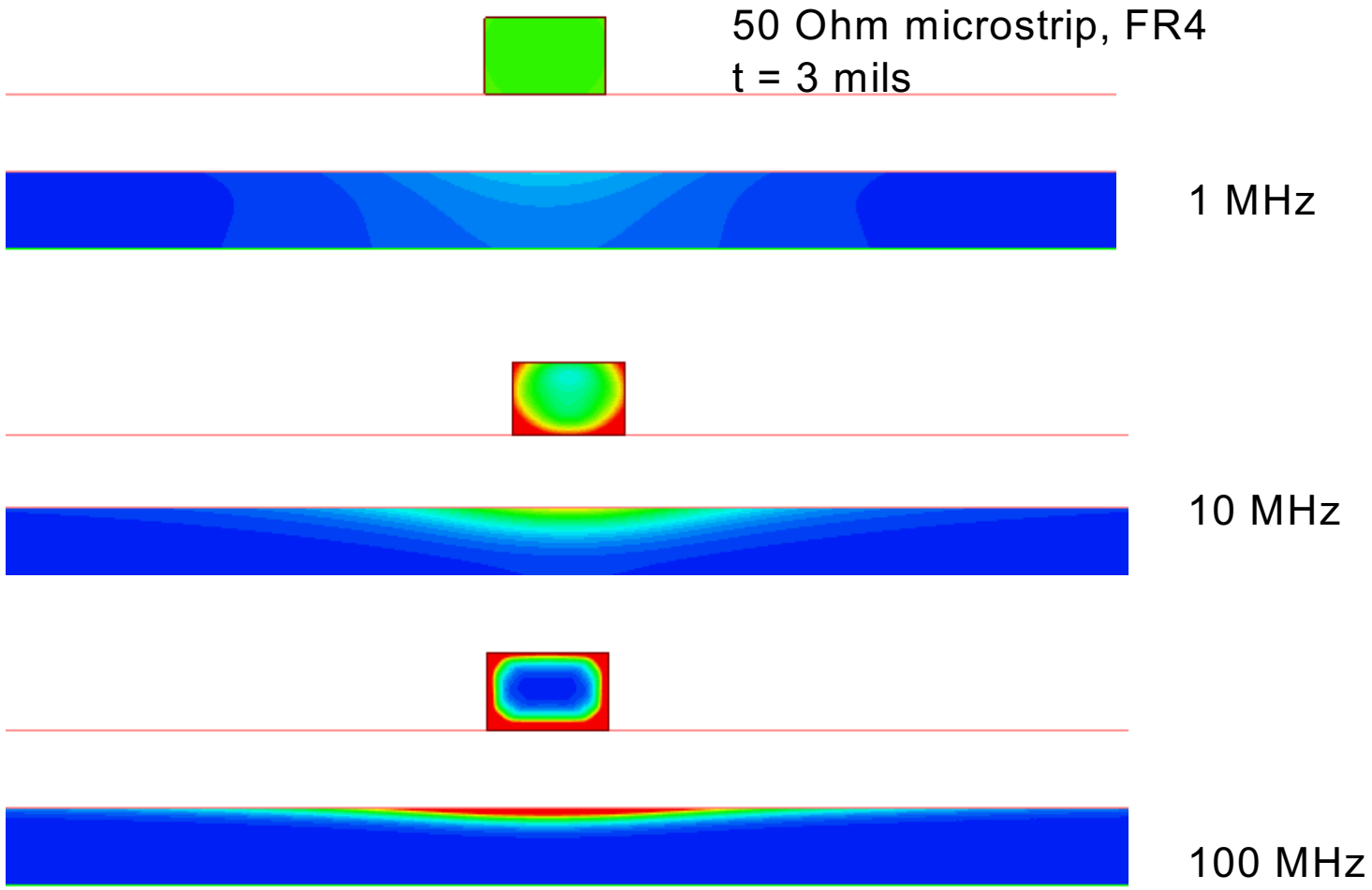
Smaller the loop area, lower the inductance

@ > 1 MHz, $\omega L > R$, path dominated by inductance

f > ~ 1 MHz



Above ~ 100 kHz, Return Current Flows Underneath Signal Current



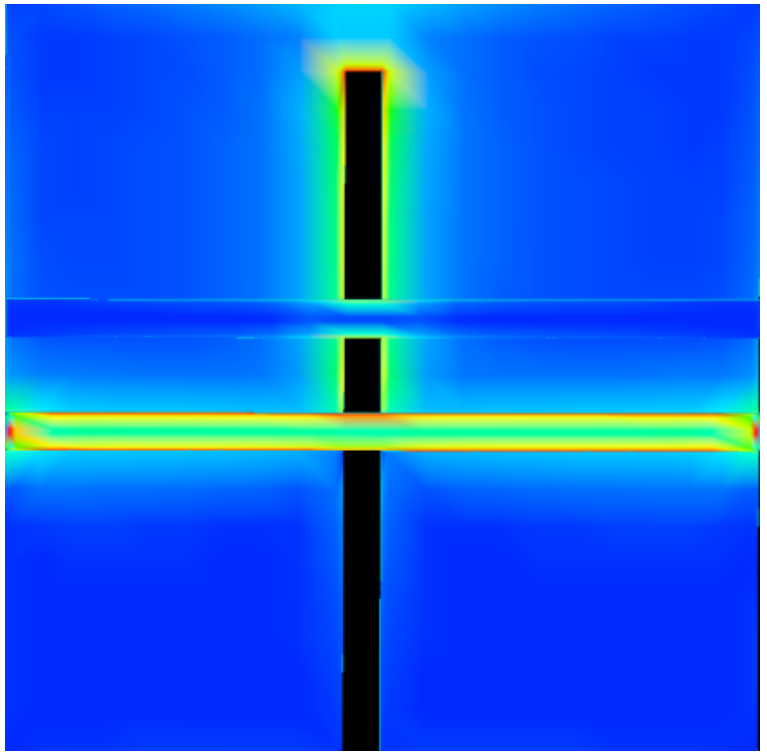
As the signal routes over the top layer, the return current follows in the plane below

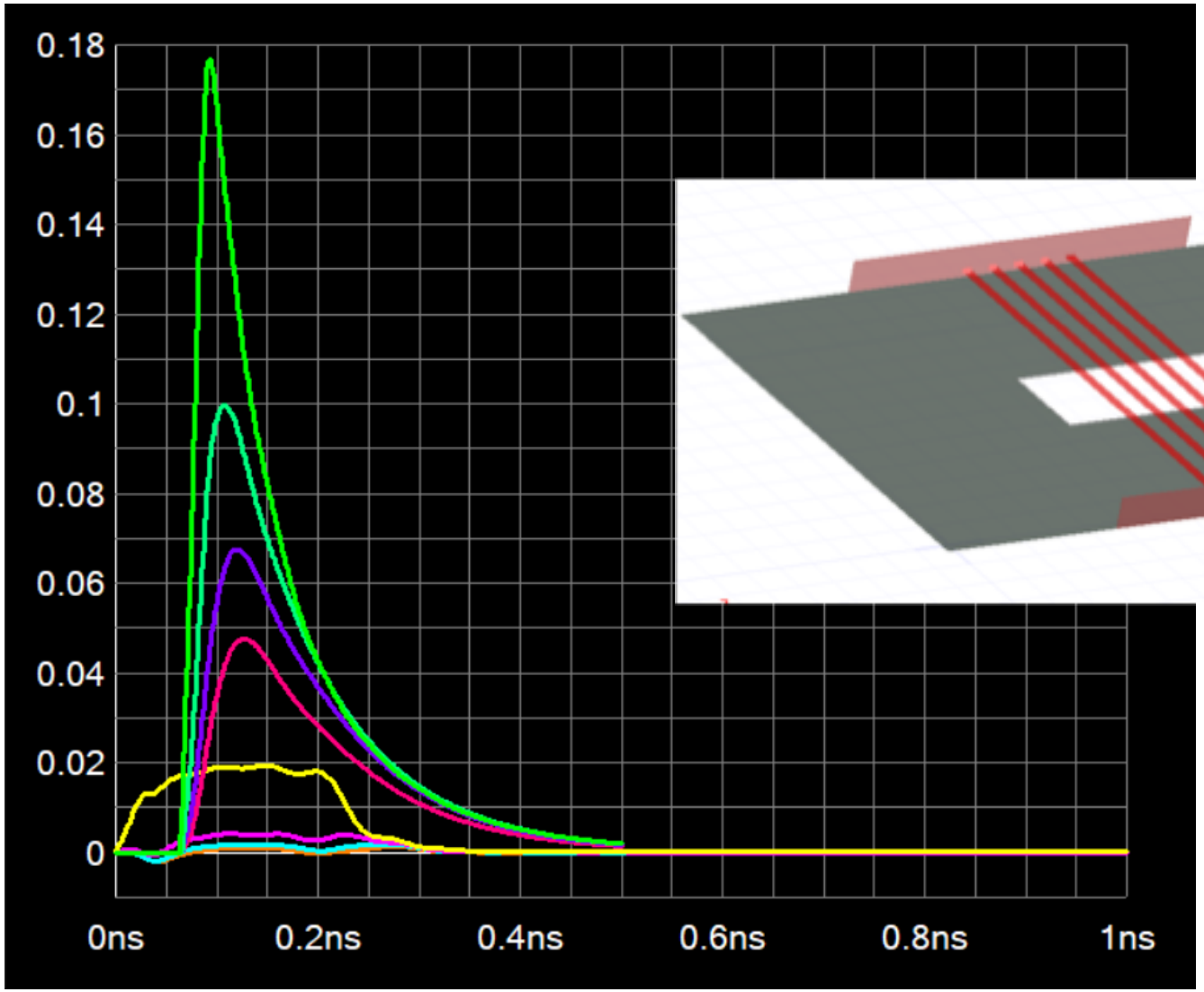
What if the Return Path is Not Continuous?

- Any non-continuous return path is a “discontinuity”, it is a screwed up return path- higher loop inductance, higher mutual inductance to other signal-return path loops

- Two consequences:
  - “self” aggression noise- a discontinuity, small impact in most of our designs
  - “mutual” aggression noise- cross talk- can be large

- Mutual aggression noise arises when:
  - Multiple signals have their return currents distorted and overlap
  - Cross talk is dominated by inductive cross talk
  - Will grow with number of signals crossing discontinuity, shorter rise times, larger discontinuity

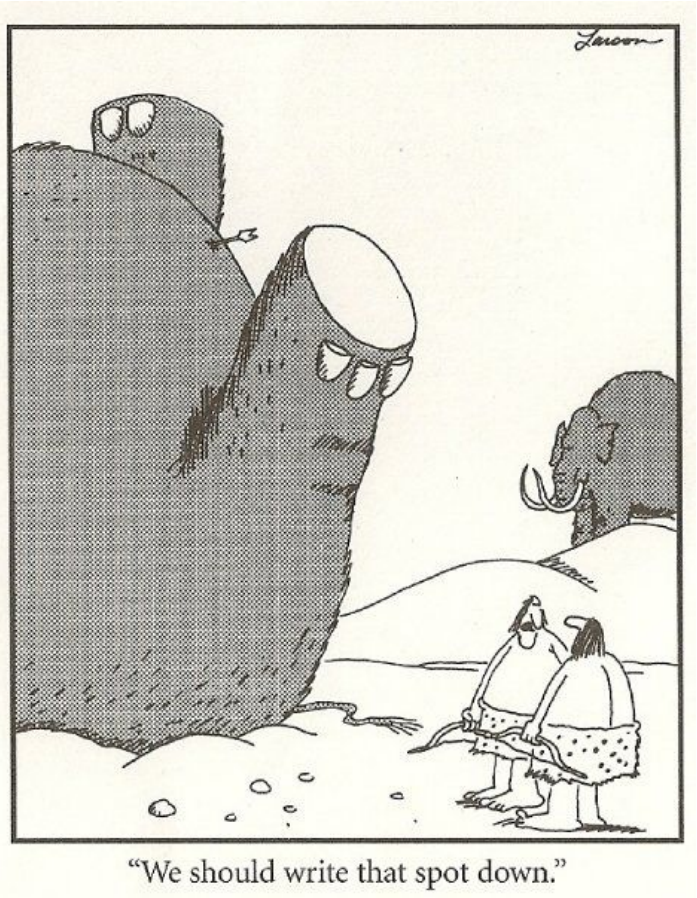




- HFSS simulation
- 5, 50 Ohm transmission lines
- Small gap, 18% cross talk!, !
- ~ 0.5 nH common path inductance

Bottom Line: Never Overlap Return Paths (Don't Cross the Streams!)

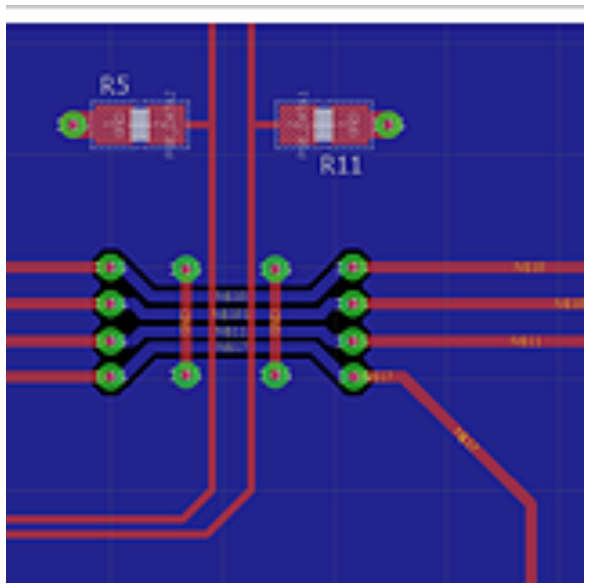
- Egon: Don't cross the streams.
  Peter: Why?
  Egon: It would be bad.
  Peter: I'm fuzzy on the whole good/bad thing. What do you mean "bad"?
  Egon: Try to imagine all life as you know it stopping instantaneously and every molecule in your body exploding at the speed of light.
  Raymond: Total protonic reversal.
  Peter: That's bad. Okay. Alright, important safety tip, thanks Egon.
- Ghostbusters

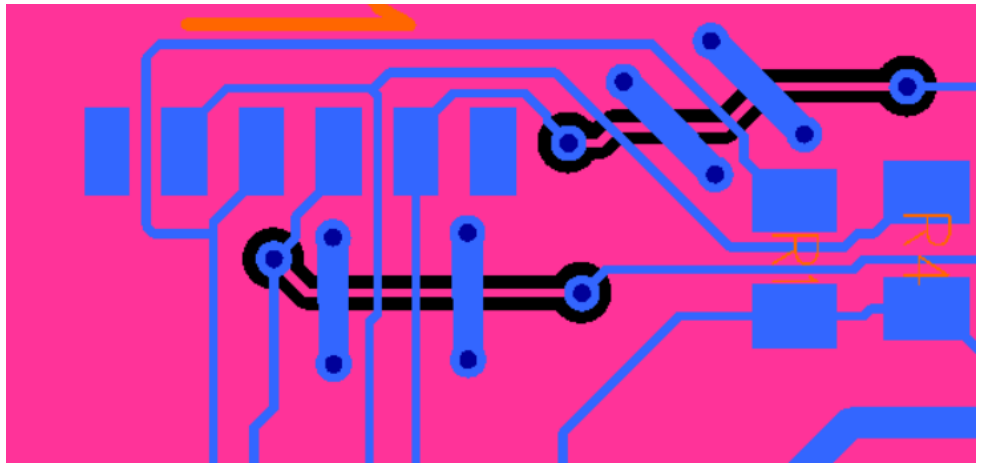


"We should write that spot down."

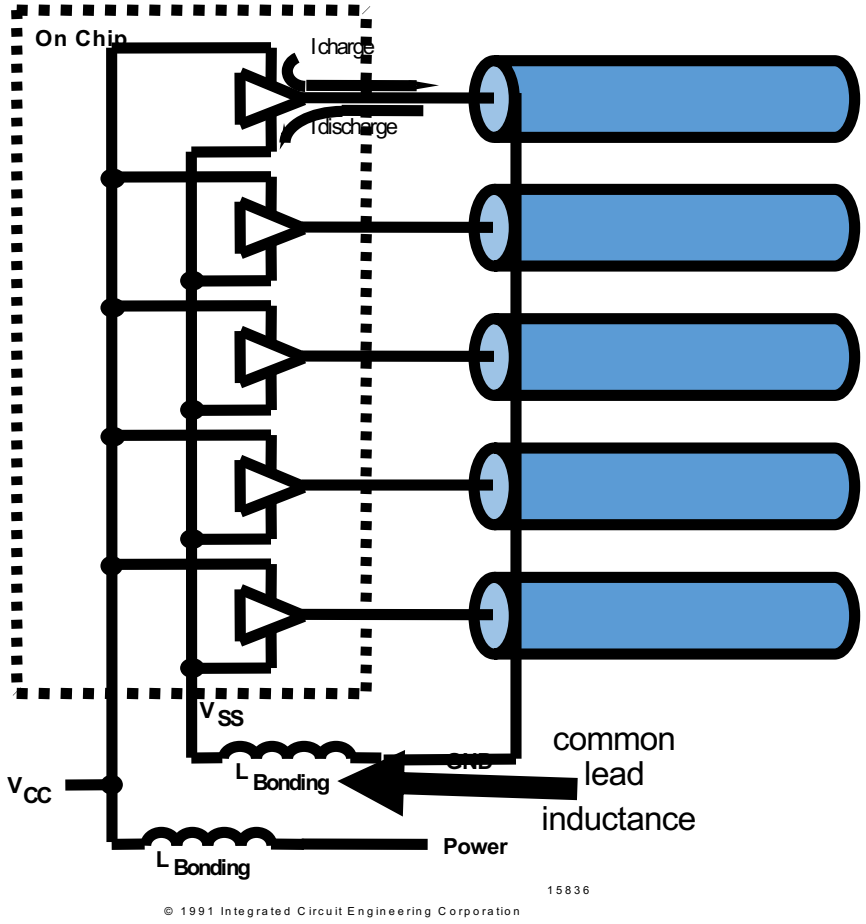
Consequences for Routing and Layout

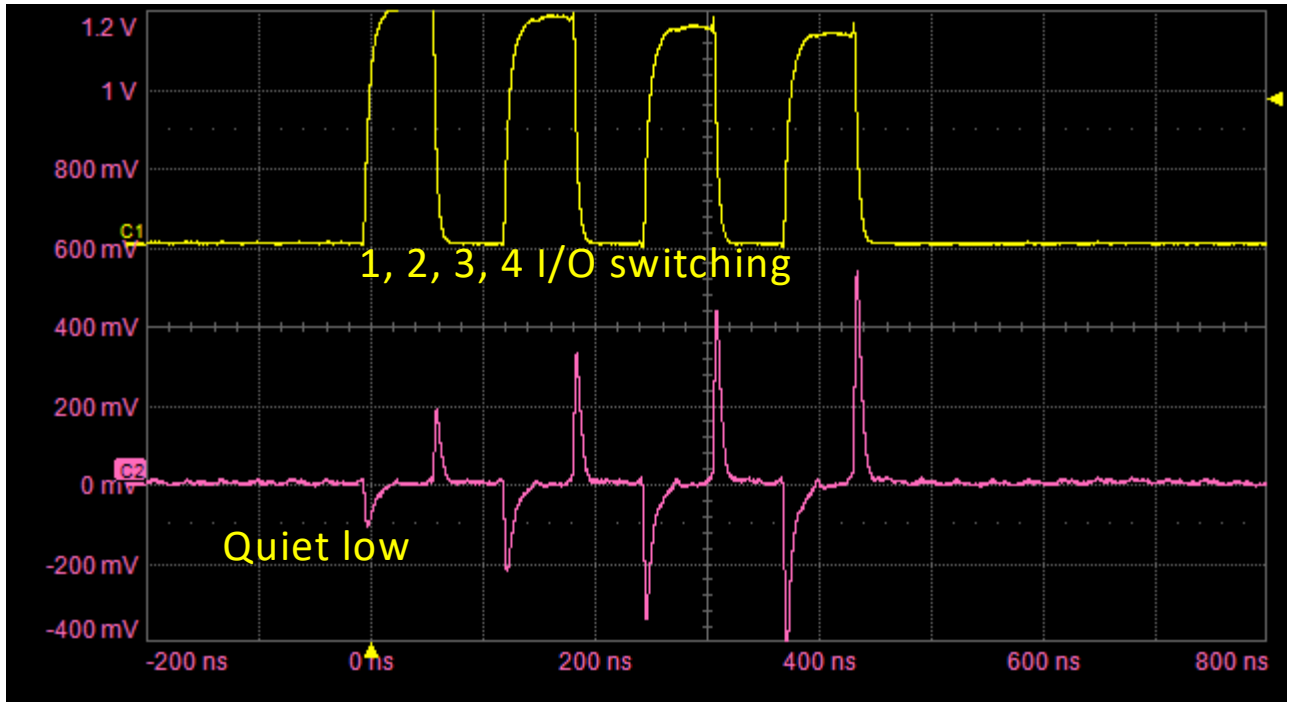
- Always use a continuous return plane under the signal line as a wide, uniform return path
- If there is a gap, due to a cross under:
  - Route around the gap: better to be longer with uniform return path than shorter with a gap
  - Cross the gap, but add adjacent return straps to provide adjacent return path





Another Source of Ground Bounce: Common Lead Inductance in Packages



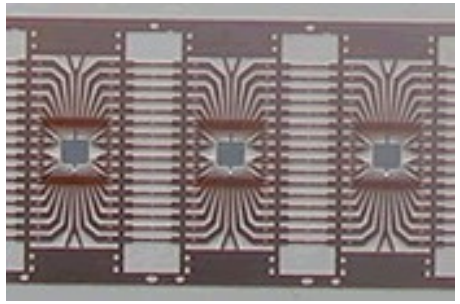


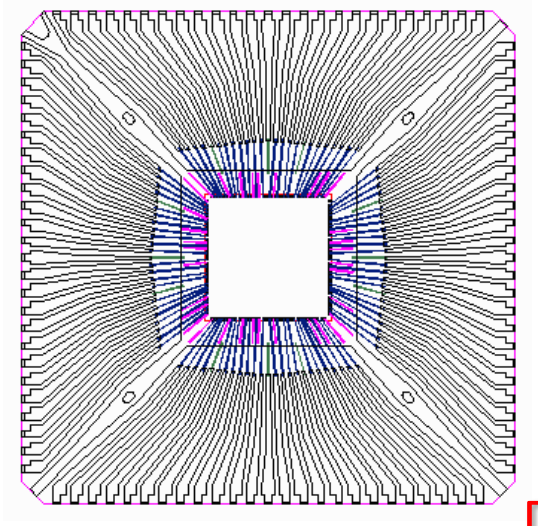
Ground Bounce Scales with the Number of I/O Simultaneously Switching and Sharing the Same Return Path

Note: differential signaling can dramatically reduce ground bounce

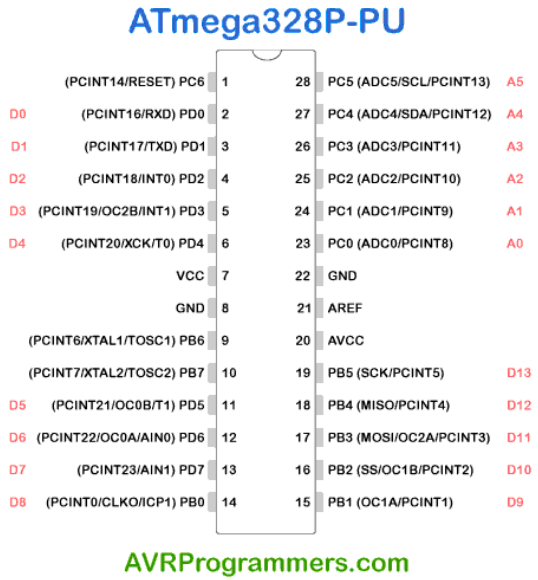
Gnd Bounce in Packages

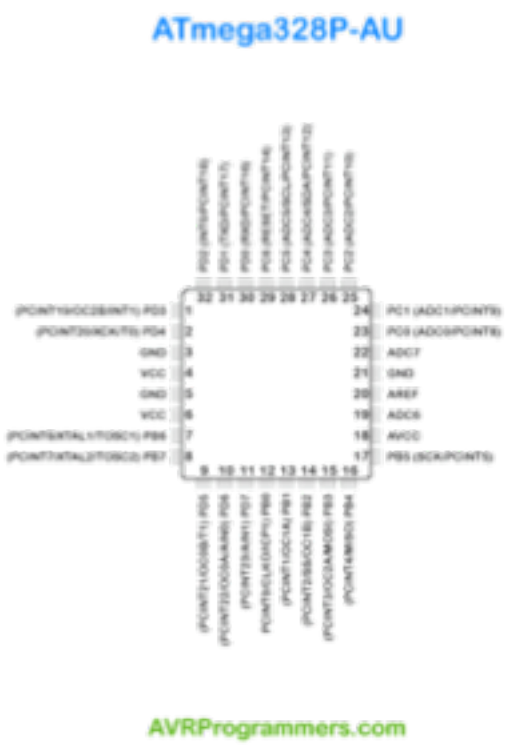
Why will these leaded packages show ground bounce?





Which pins should be selected as pwr/gnd?



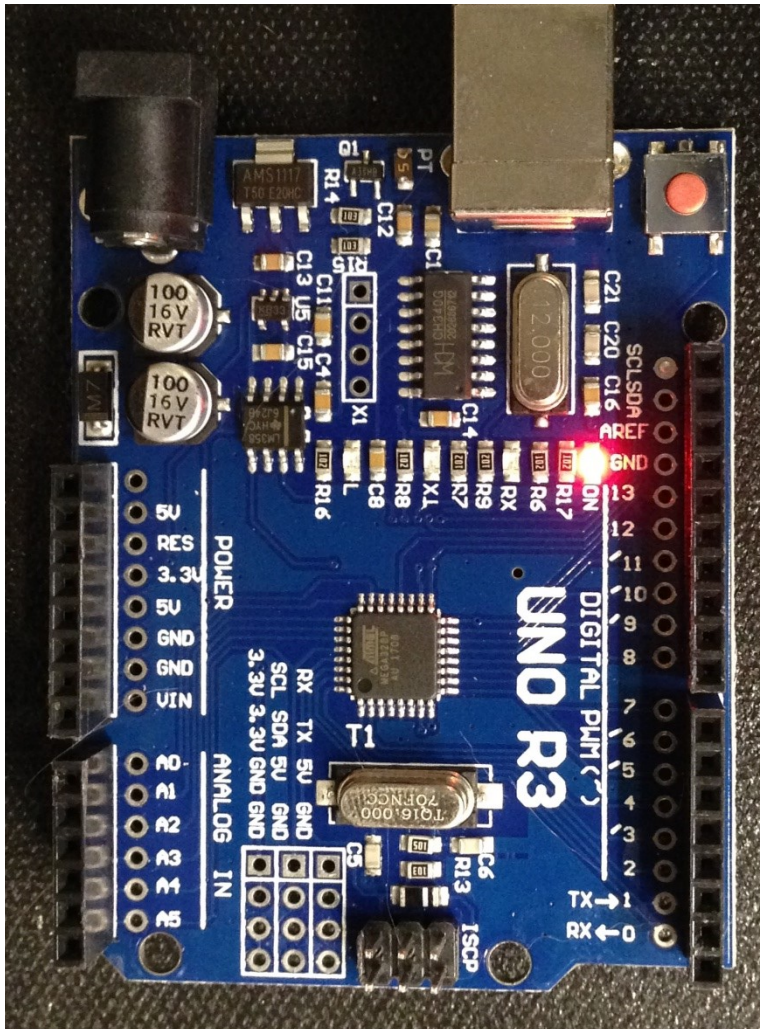


Don’t make it worse!

Keep the path from package gnd pin to the return plane short and wide

Consequences for Routing and Layout

- Always use a continuous return plane under the signal line as a wide, uniform return path
- If there is a gap:
  - Route around the gap: better to be longer with uniform return path than shorter with a gap
  - Cross the gap, but add adjacent return straps to provide adjacent return path
- Connecting to an IC, other components
  - Keep gnd connections as short, wide as possible to the return plane- drop a gnd via as close to IC pin as possible.
  - Consider routing inward, under package to a via to the bottom ground plane
- In connectors
  - Keep adjacent return pins to every signal pin (may mean more pins in connector)
  - Keep number of signals sharing the same return to a minimum
  - An Arduino board is the worst configuration you can engineer: where are the return pins for the digital I/O?



In Reality, We Play the Whack-a-Mole Game in Every Design

Every application has a different set of tradeoffs

"Engineering is Geek for tradeoff analysis"
- Bruce Archambault

Performance

Cost
Schedule
Risk

Fundamental tradeoffs:

- Higher performance → higher cost
- Lower cost → higher risk
- Pulled in schedule → higher risk and higher cost
- Longer rise time, less noise → worse timing, worse performance
- Reduce cross talk → lower impedance
- Lower impedance → higher power consumption
- Higher interconnect density → higher cross talk
- Tighter diff pair coupling → higher loss

Risk Reduction is Key to the Design Process

- Many designs may “work” just fine not following the best design practices (reinforces bad habits)
- They may work ***in spite of*** the layout, but your next design might not
- If you are not going to simulate (and have confidence your process will find ALL the noise problems), you need to buy insurance
  - Following ***best design practices*** is a good habit, if it does not add cost
  - Over design- pay more for larger performance margins (buy insurance)
  - The more information you have the lower your risk
- Design more like a Mom, less like a Dad

A Mom’s perspective: (great at identifying worse case scenarios)
“Be careful, you could put your eye out with that thing.”

A Dad’s perspective (a Coloradan)
“Here, hold my beer”

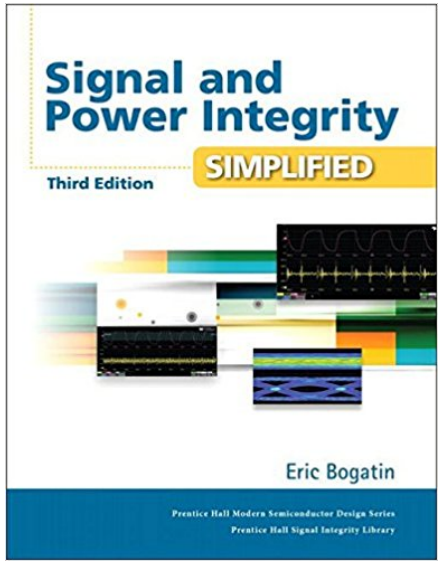
Outline: Some Perspective

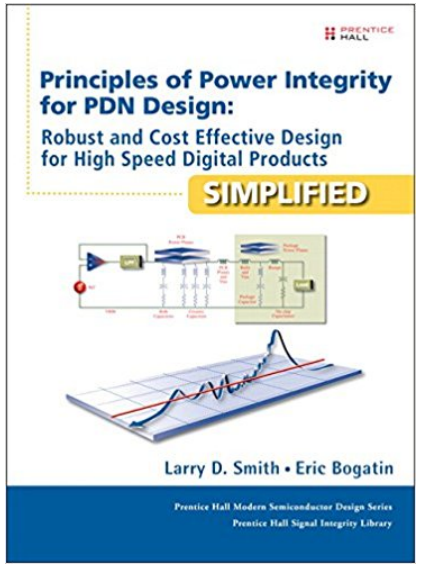
- When not to worry: if solderless bread board works, interconencts are transparent
- How to sleep better at night
- Seven Best Design Practices of highly successful designers to reduce:
  - ***Reflection noise-*** controlled Z0, terminations, routing topologies
  - ***Cross talk noise-*** uniform return planes, space out traces, stripline
  - ***Ground bounce noise-*** don't screw up the return path, don't share return paths
  - ***High speed serial links noise-*** reduce losses, engineer lower mode conversion
  - ***Power distribution noise-*** reduce L everywhere, increase C, engineer damping
  - ***EMI noise-*** reduce ground bounce, use 360 degree connectors, shield

  - *Going forward*

A Practical Strategy

- Follow Best Design Practices (unless you have a strong compelling reason otherwise)
  - Based on many assumptions!
  - Try to understand the underlying assumptions
- Take every opportunity to move up the learning curve
- Empower yourself to be your own expert
  - Learn the basic principles- don't just memorize a bunch of rules
  - Learn to make your own tradeoffs
  - Read text books
  - View online classes
  - Attend webinars
  - Visit conferences and their tutorials
- Question authority- not all the information out there is good information! Follow good curated sources





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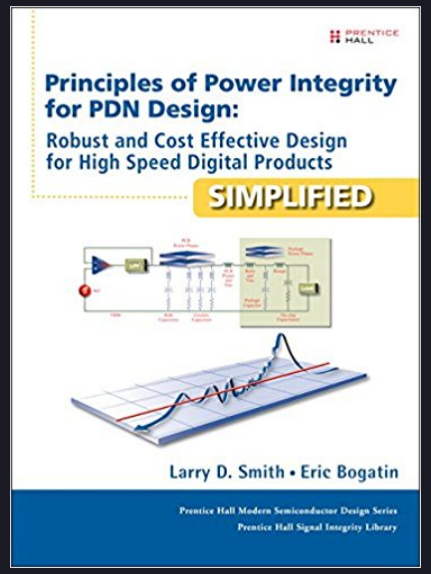

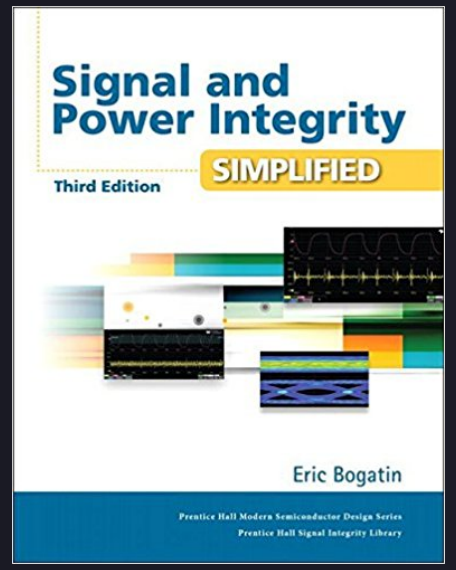

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