

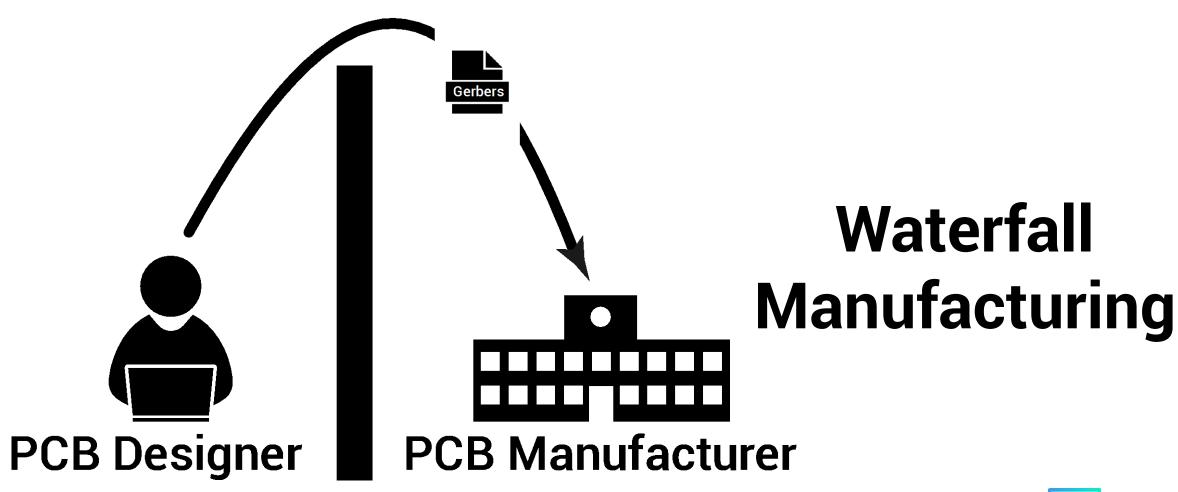
### Agenda

- (1) Waterfall Manufacturing
- (²) Agile Manufacturing
- (3) Best Practice 1: Design Intent Synchronization

Altium.

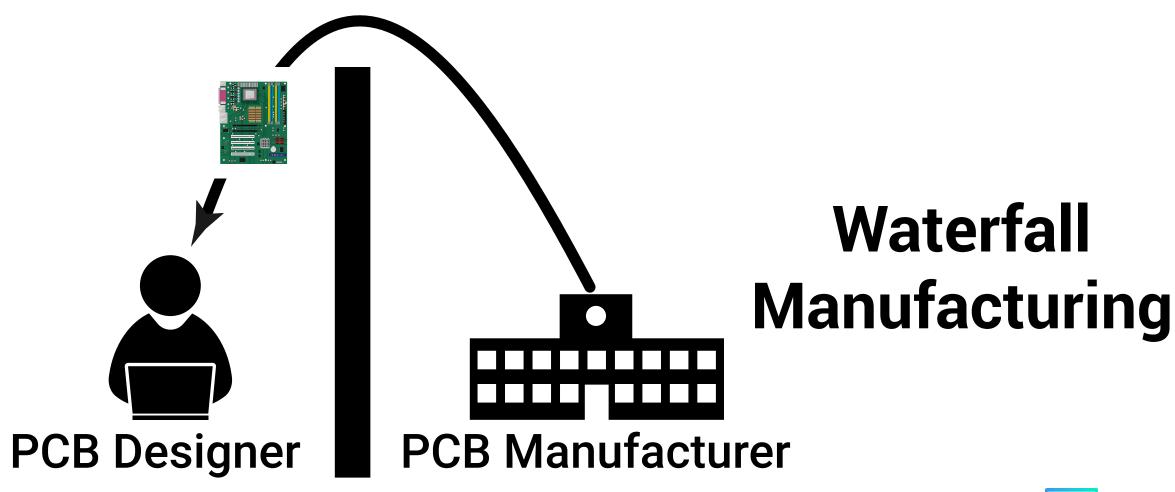
- Best Practice 2: Quote Optimization
- Best Practice 3: Manufacturing Synchronization
- (6) Best Practice 4: Transfer Manufacturing Knowledge







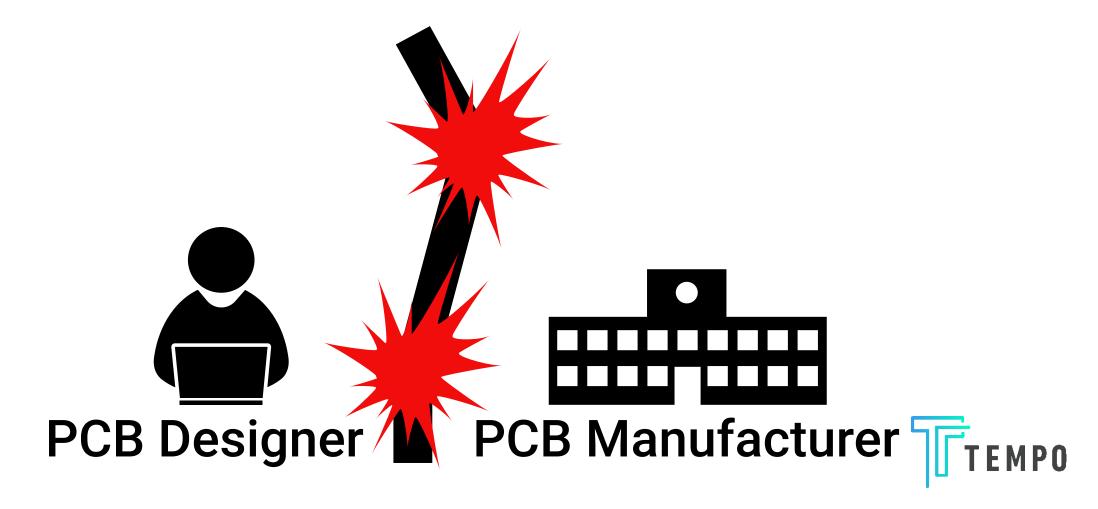








### **Shatter the Wall**



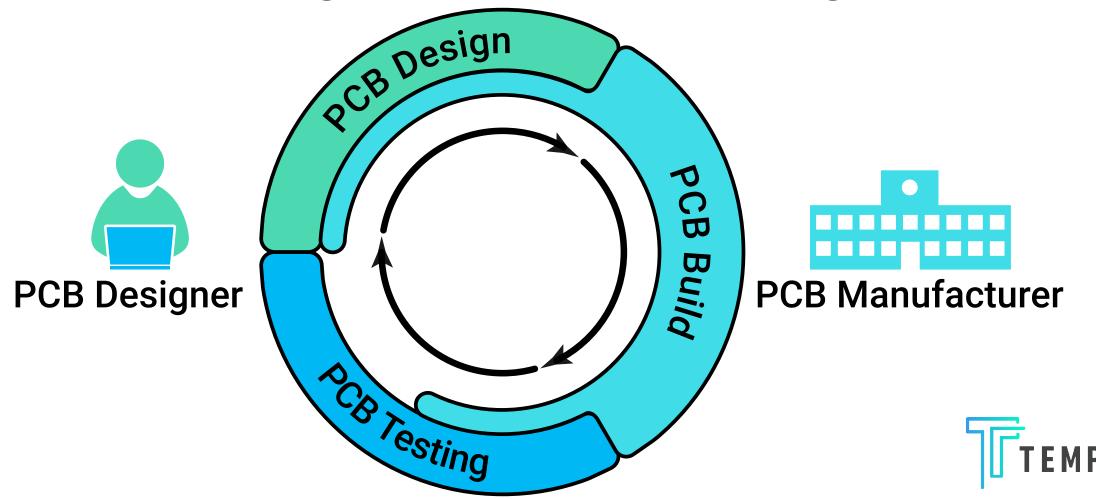


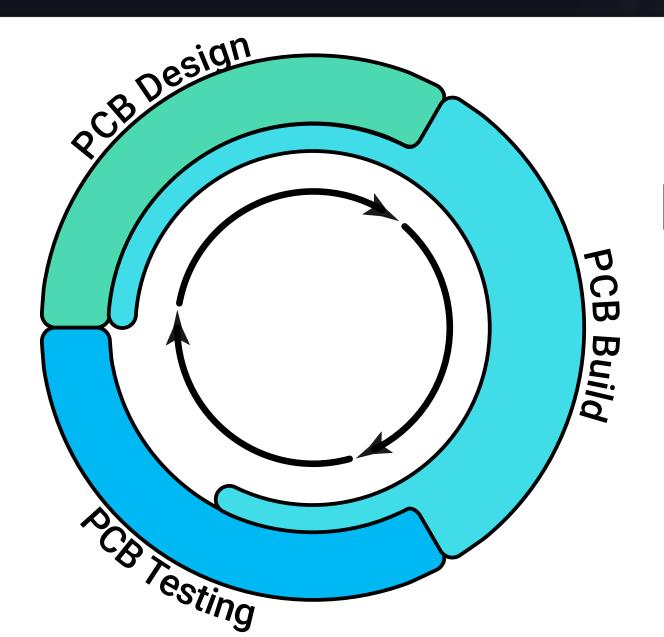
### From Waterfall Manufacturing...





### ... to Agile Manufacturing

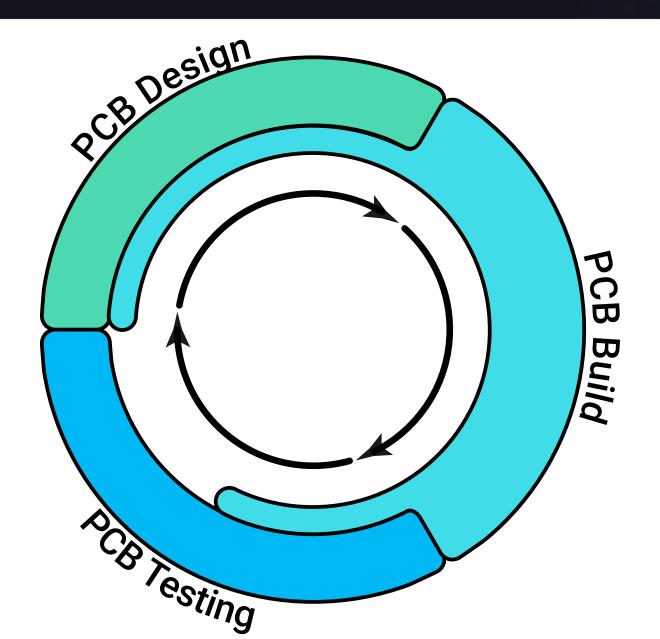




# How do you achieve Agile Manufacturing?





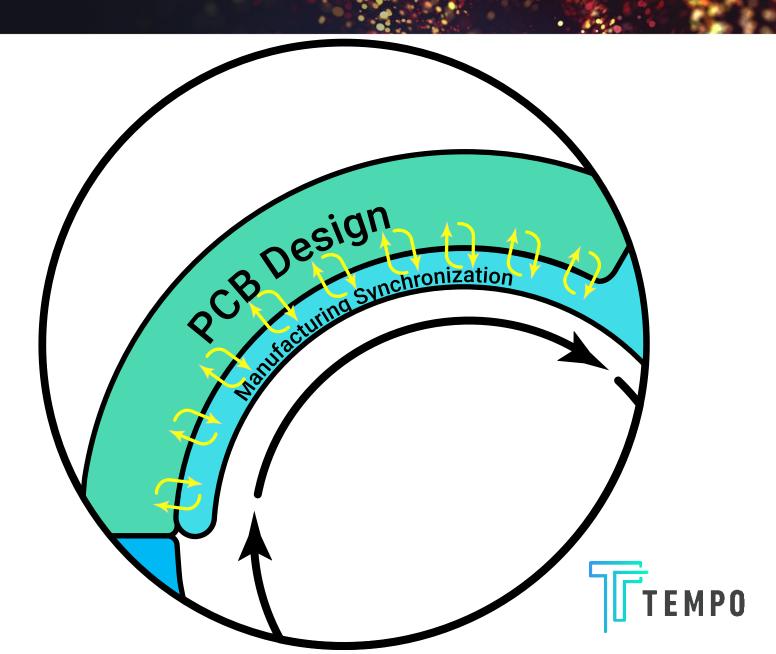


### Radical Transparency!



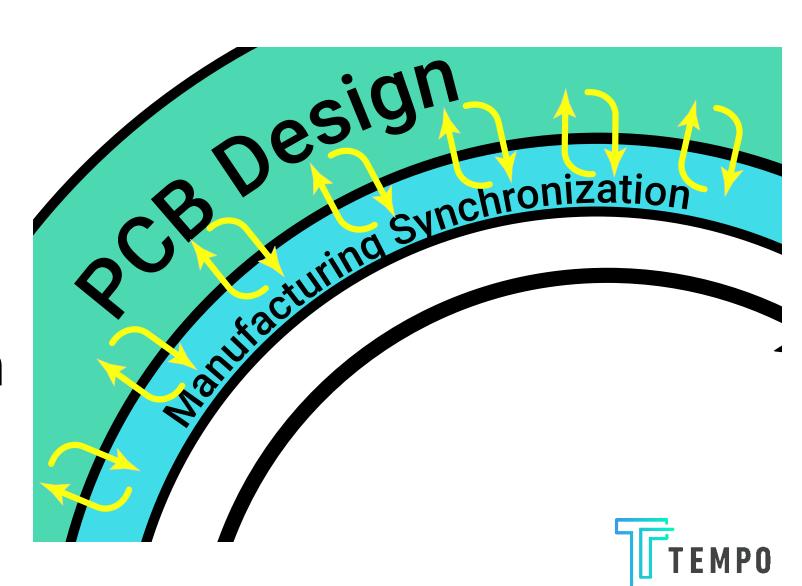


## Transparency during PCB Design





### Best Practice 1: Manufacturing Synchronization



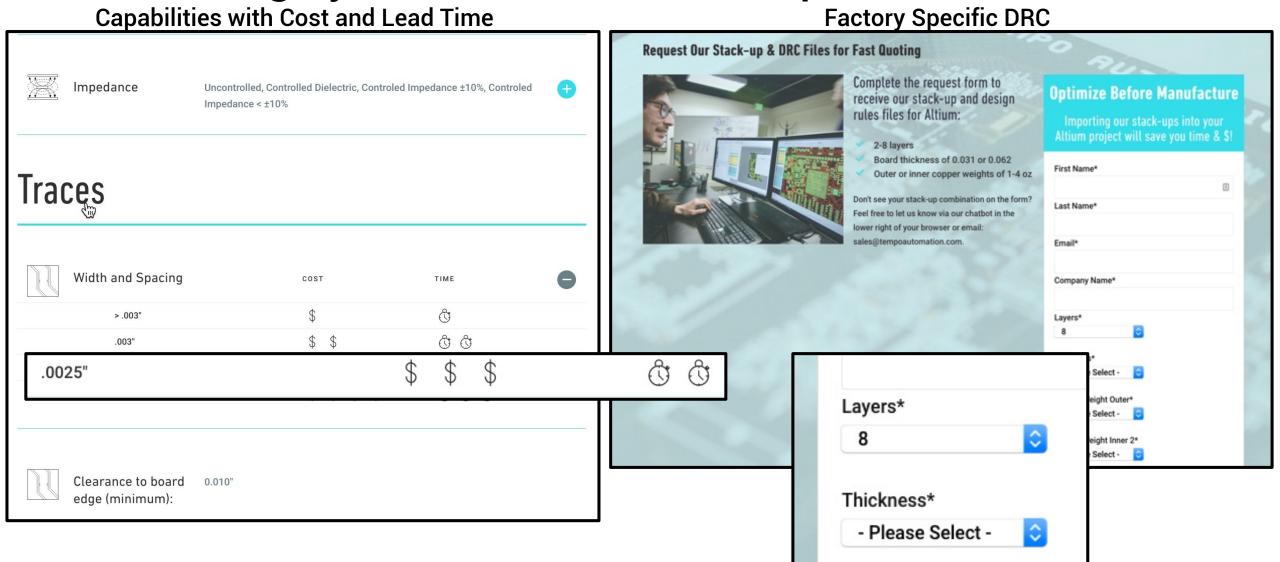


### **Manufacturing Synchronization Best Practices**

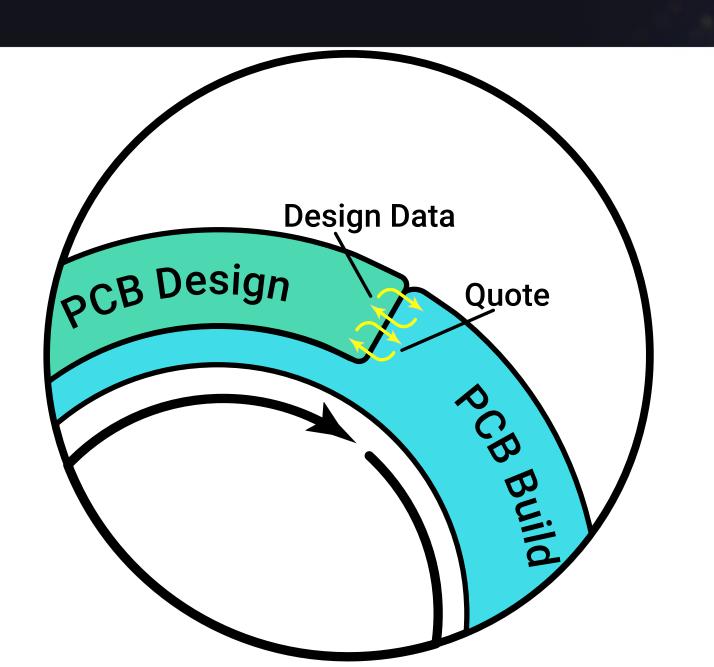
| Planning  | <ul> <li>Engage with CM</li> <li>Confirm CM supports QC requirements</li> <li>Determine special processes required</li> <li>Generate target stackup</li> </ul> |
|-----------|--|
| Sourcing  | <ul> <li>Compile for component sensitives</li> <li>Check for stock availabilities</li> </ul>   |
| Schematic | <ul> <li>Include features for testing at CM</li> </ul>   |
| Layout    | <ul> <li>Use DRC rules specific to the CM</li> <li>Check thermal impacts of manufacturing</li> </ul>   |



Manufacturing Synchronization with Tempo





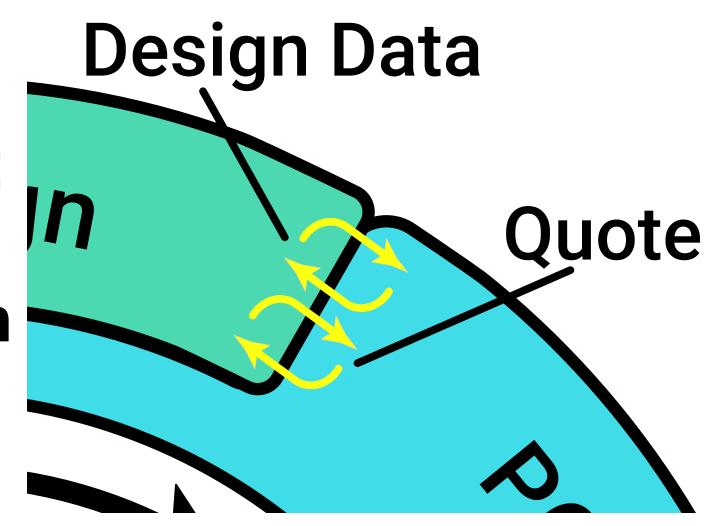


# Transparency during transfer to PCB Build





# Best Practice 2: Design Intent Synchronization





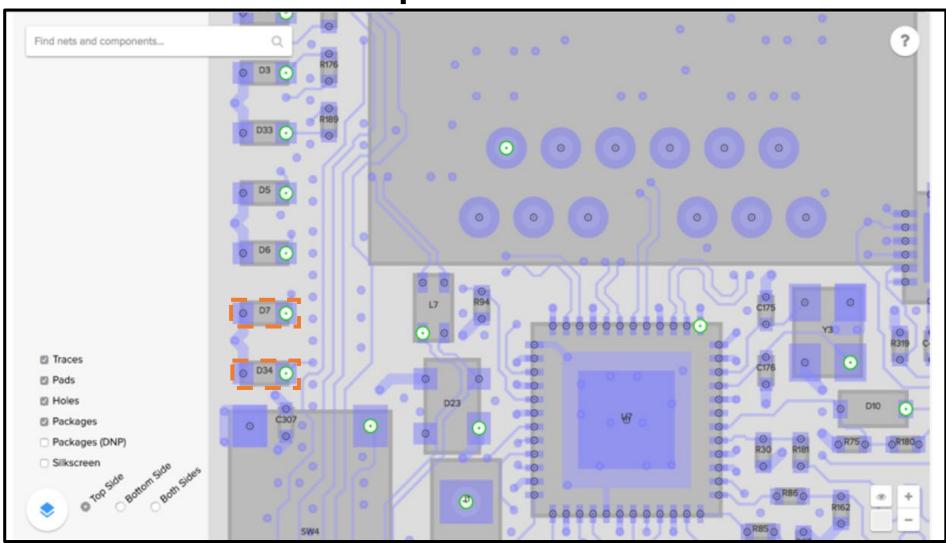


### **Design Intent Synchronization Best Practices**

| = 33.9  |   |  |
|---------|---|--|
| CAD     | <ul> <li>Gerbers are incomplete, use native CAD or IPC-<br/>2581</li> </ul> |  |
| ВОМ     | <ul><li>Use CM supplied template</li><li>Simulate procurement</li></ul>     |  |
|         | <ul> <li>Check for CAD – BOM mismatch</li> </ul>                            |  |
| Stackup | Iterate implementation with manufacturer                                    |  |
| Notes   | <ul> <li>Confirm receipt and understanding</li> </ul>                       |  |

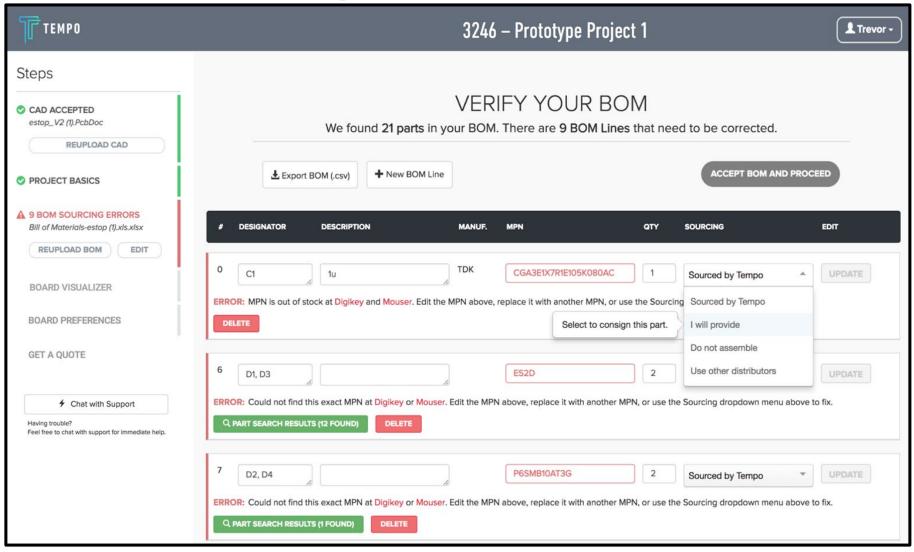


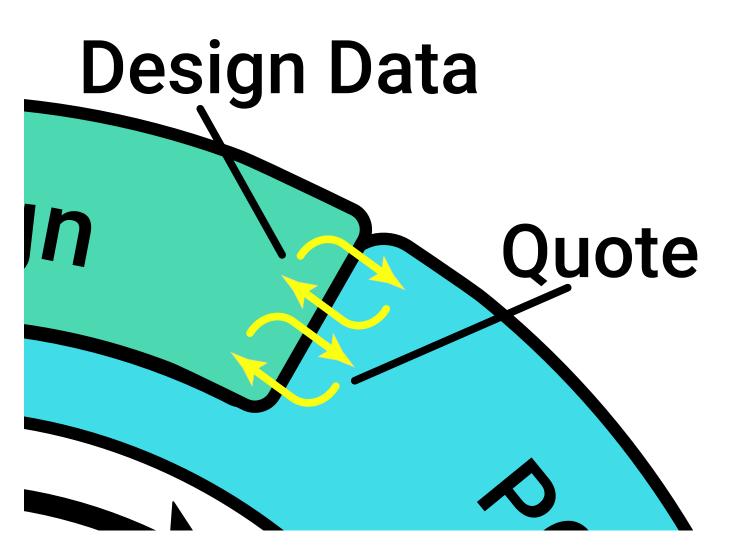
### **CAD Validation with Tempo**





### **BOM Validation with Tempo**





### **Best Practice 3: Quote Optimization**





### **Price Optimization Best Practices**

| Components | <ul> <li>Use Approved Parts List (AVL) to allow crosses</li> <li>Request component level price breakdown</li> </ul> |
|------------|---|
| Fab        | <ul> <li>Ask pricing implications for board parameters</li> <li>Maximize boards per panel</li> </ul>                |
|            | <ul> <li>TH placements 5x &gt; SMT</li> </ul>   |

Assembly

Leadless 8x > SMT





### **Lead Time Optimization Best Practices**

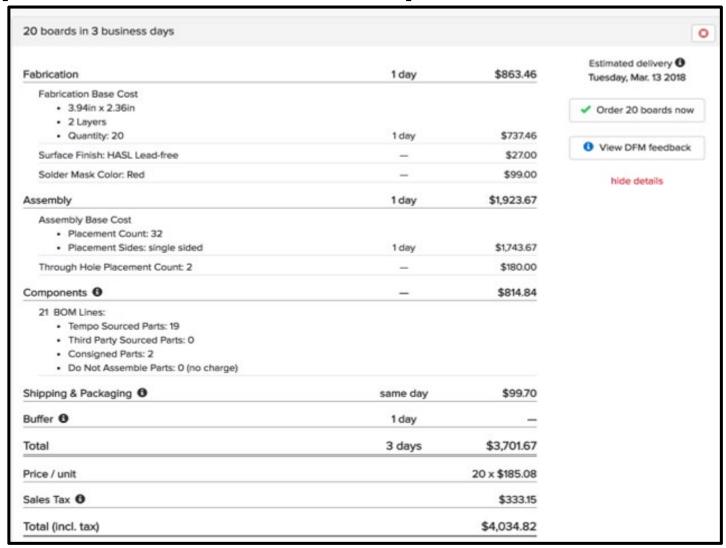
| Components | <ul> <li>Use Approved Parts List (AVL)</li> <li>Secure low stock component early</li> </ul>                    |
|------------|--|
| Fab        | <ul> <li>Minimize materials that not stocked</li> <li>Choose via type to minimize lamination cycles</li> </ul> |
|            | <ul> <li>Minimize number of through hole parts</li> </ul>  |

Assembly |

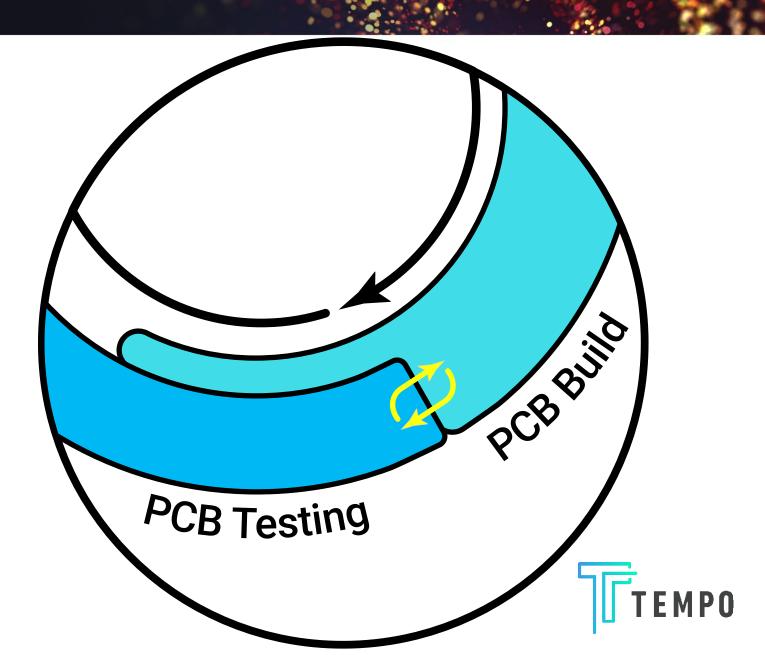
Minimize special operations (press fit etc.)



### **Quote Optimization with Tempo**

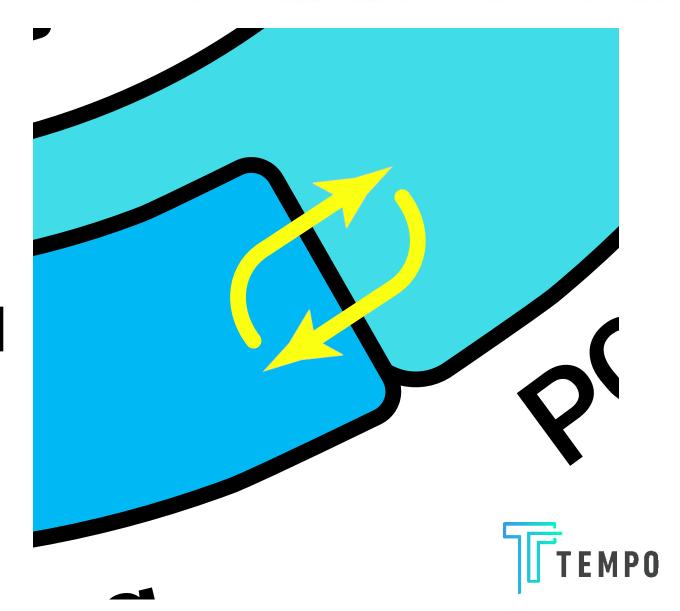


Transparency during transfer from PCB Build





### Best Practice 4: Learn from each Build





### **Knowledge Transfer Best Practices**

| Files    | <ul> <li>As built production files</li> <li>Design recommendations</li> </ul> |
|----------|---|
| Programs | <ul><li>Reflow profile</li><li>Machine programs</li></ul>                     |
|          |   |

DiagnosticsProduction logQA records



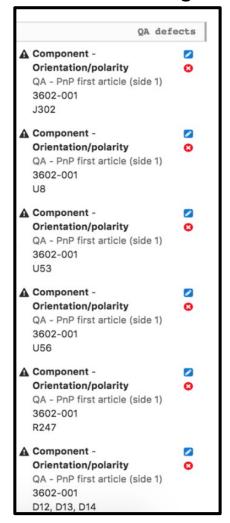


### **Knowledge Transfer with Tempo**

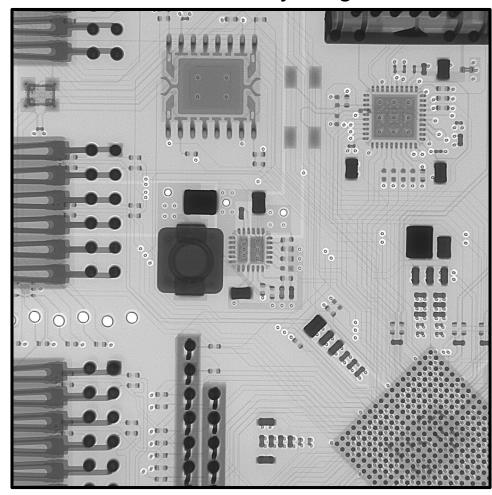
### **Traveler Traceability**



#### **Production Log**

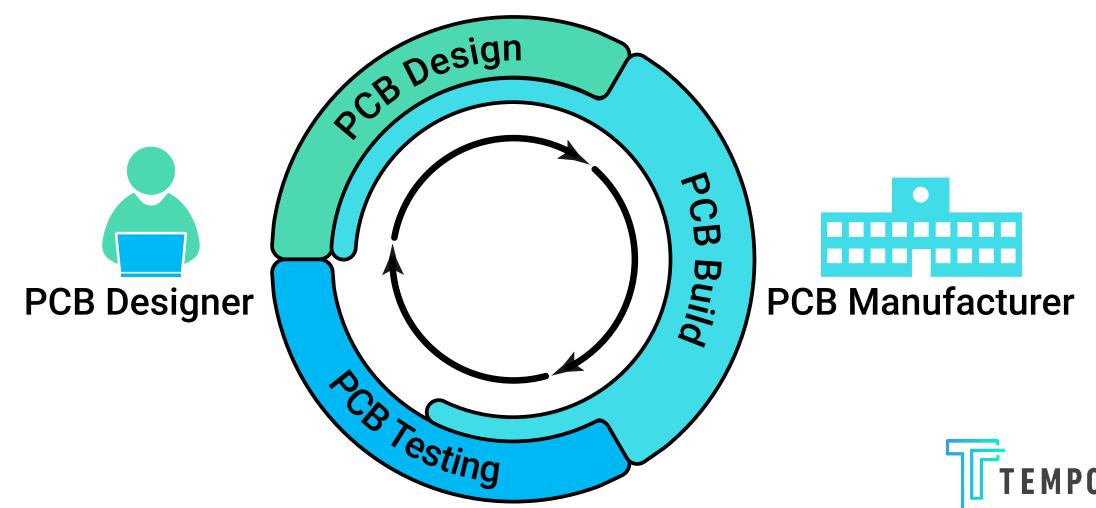


#### **AOI** and X-Ray Image





### **Agile PCBA Manufacturing**





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