Altium

Getting the Layer Stack Right

Christopher E. Carlson

Sr. Field Applications Engineer

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INTRODUCTION

One of the most common mistakes during the PCB fabrication process is improper layer order. If left unchecked, it can cause the whole process to fail. The PCB assembly process may function from an electrical continuity standpoint. It may even pass an electrical inspection. However, in designs in which the order of plane to signal layer, and the proximity of layers with respect to each other is paramount, failures will occur at the final functional assembly level.

In order to guarantee that the fabricator has the required information to order the layers properly and perform a post-process visual inspection, details must be engineered directly into the copper geometry. It is the responsibility of the PCB designer to include these copper features in the design.

Designing the proper copper features into the fabrication data provides a high degree of confidence that the proper layer stackup order will be achieved. Additionally, these copper features provide a mechanism for the inspection of the final assembly, once it undergoes an in-house Q&A inspection and has been cleared to go to the fabrication house.

LAYER IDENTIFICATION

The first feature added to the copper on each layer identifies the layer order with respect to all other layers. Each layer receives a layer number, etched directly into the copper, which indicates its position within the layer stackup. It is not enough to place the layer numbers outside the board outline to indicate which layer the artwork plot is intended for. The layer numbering must be incorporated within the area of the finished board.

Some fabricators will require the layer number for the secondary side layer to be mirrored. The layer number should be located near the edge of the board so as not to interfere with the electrical properties of the circuit. It can take the form of a single number on each layer.

However, the numbers may not be stacked on top of each other. They must all be clearly visible when viewing the check plots from the top down, when all of the check plots are stacked on top of each other.

To make them even easier to identify, layer numbers are often placed inside of a rectangular box. Soldering masks and silk screen features must be removed from the area surrounding the layer numbers, in order to facilitate viewing of the layer numbers through the finished PCB with an inspection light source placed behind the assembly. The layer numbers will be an indication that all of the layers are present. Additionally, it will give the fabricator an indication of which layer the artwork plot is intended for.

Layer numbers must not connect to copper features, such as power planes or polygons, on any layer. If necessary, power planes and polygons must be indented where layer numbers are plotted to increase the spacing to at least 0.010" between the plane or polygon features and the layer numbers.

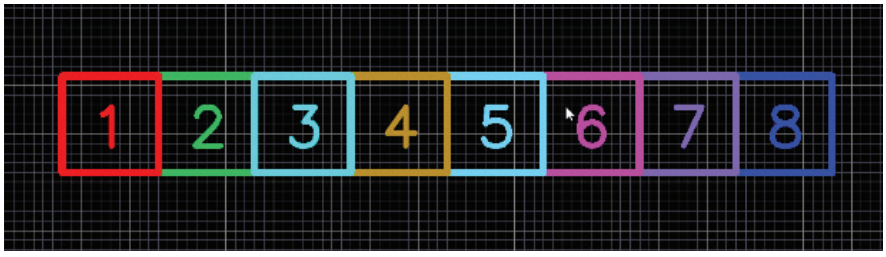

Figure 1: Layer numbers etched into the copper geometry for each layer.

Figure 2: Layer numbers showing the removal of solder mask for visual inspection.

STACKING STRIPES AND TEST TRACES

Stacking stripes are copper features that are placed on the edge of the PCB, to facilitate visual inspections of the layer order. The geometry must extend outside the board edge in order to expose the copper when the PCB is routed from the panel. By observing the stacking stripes on the edge of the finished board, the proper stackup geometry will be visible. The stacking stripe is `50 mils` wide by `200 mils` long on layer 1, and is `100 mils` longer on each subsequent layer.

The objective of the test trace is to verify the post etch copper thickness and width on each layer in the stackup. Test traces are `50 mils` long by `5 mils` wide and must extend outside the board edge in order to expose the copper when the PCB is routed from the panel. The edge view of a test trace can be measured with an inspection microscope. This feature is paramount in designs with impedance-driven geometries.

Much like layer number, stacking stripes and test tracks must not connect to copper features such as power planes or polygons on any layer, and must be indented to increase the spacing to at least `0.010"` between the plane or polygon features and the stacking stripes or test tracks.

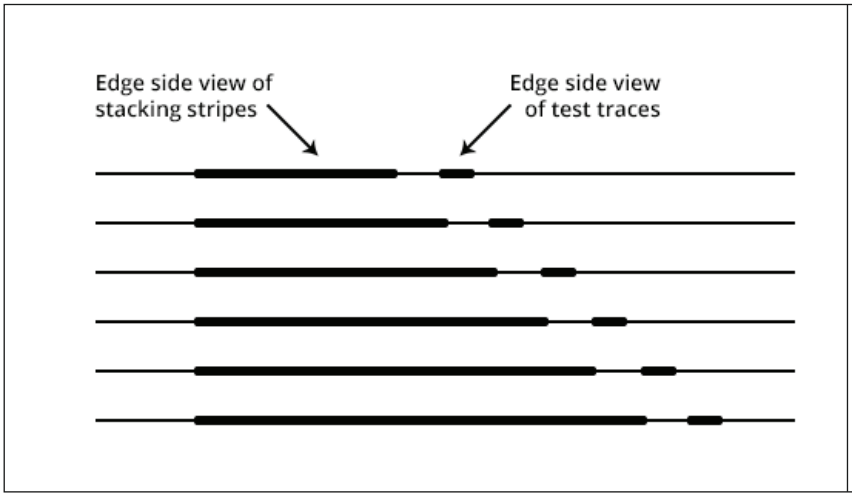

Figure 3: Edge view of stacking stripes and test traces.

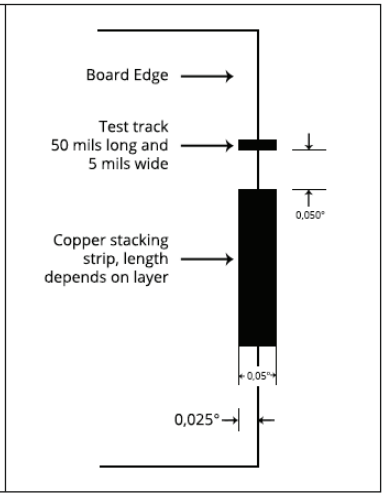

Figure 4: Stacking stripe dimensions and test traces as plotted on film layers.

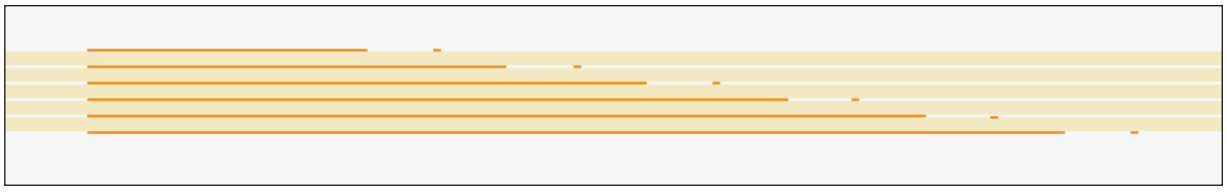

Figure 5: Edge view of stacking stripes and test traces

CONCLUSION

You can achieve a high degree of confidence in your layer stackup, if you make good use of layer numbers and stacking stripes. These features are engineered into the PCB assembly in the early stages of the design. Considerations for the necessary real estate and electrical clearance must be taken into account during the PCB layout planning stages.