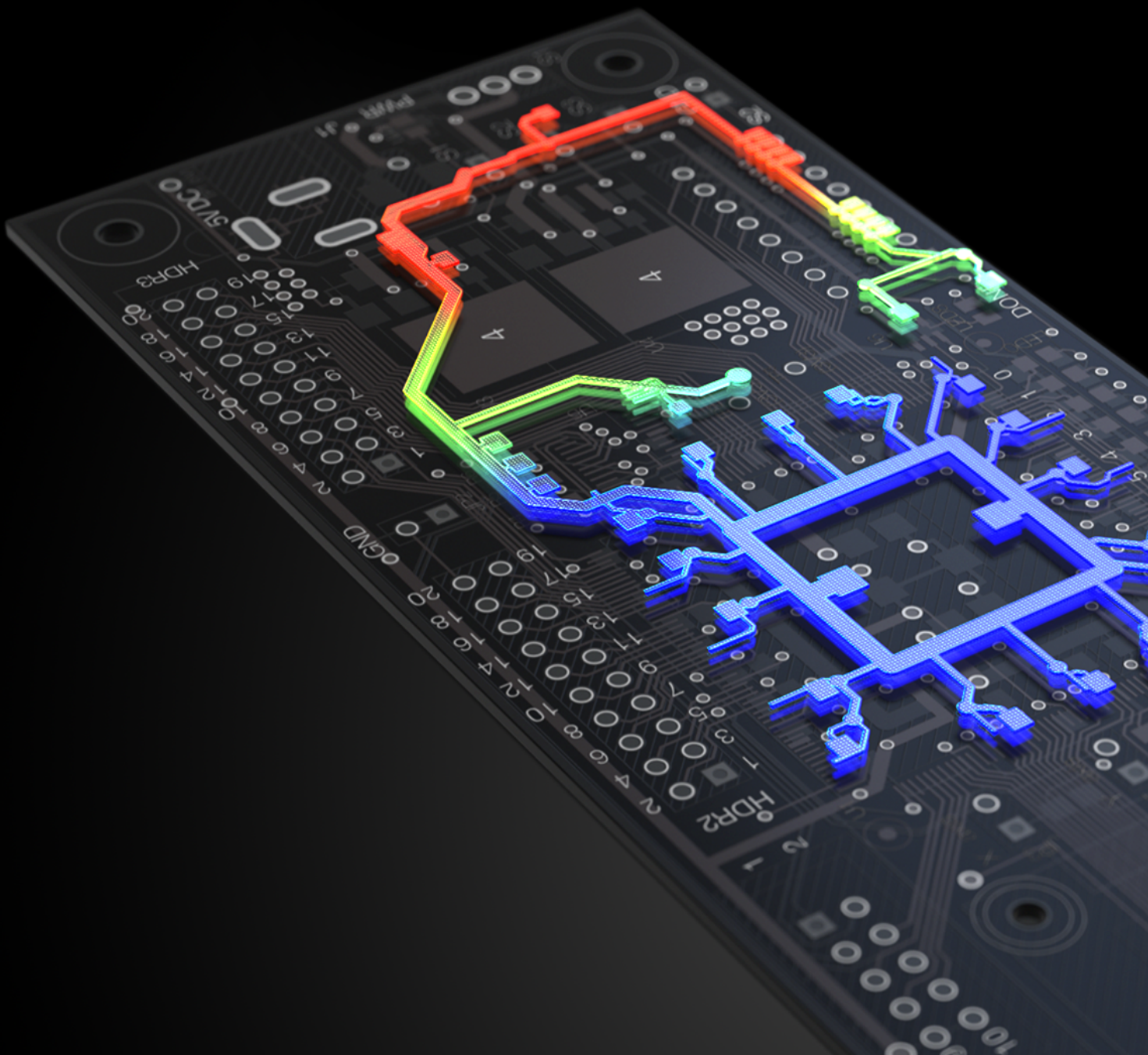
Altium®

Getting Started with PDN Analyzer



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GETTING STARTED WITH PDN ANALYZER

Your Power Distribution Network (**PDN**) operates as your design's circulatory system. You want to discover complications before they become real problems. Rather than treating **PDN** issues as a post-design afterthoughts to discover with physical prototypes, you need a way to accurately identify and resolve **PDN** issues at design time, not after. With **PDN Analyzer powered by CST®** in **Altium Designer®**, we've made **PDN** analysis an approachable and intuitive process for every PCB designer, regardless of their experience level. Inside this demonstration guide we'll guide you step-by-step through an initial **PDN Analyzer (PDNA)** setup, so you can become comfortable with optimizing your **PDN** at design time without ever relying on a physical prototype.

PDN Analyzer delivers the following benefits to your design process:

Visual Power Analysis

- Easily identify and resolve DC voltage and current density issues during your board layout process with no prior experience necessary.

Unified Design & Analysis Environment

- Analyze - Modify - Analyze - without ever interrupting your design workflow.

Simultaneous Multi-Network Simulation

- Calculate network and return paths and their interactions that simple batch simulation can't provide with true **Voltage Regulator Models** (**VRMs**).

Configurable HTML reports

- Provide a record of your simulation work, including sortable tables with voltage and current margins, power consumption data, and custom screenshots.

Product Reliability at a Lower Cost

- Ensure the correct performance of individual supplies within the design, in terms of standing voltage levels, voltage stability, and trace heating/damage without overdesigning.

Improved PCB Layout

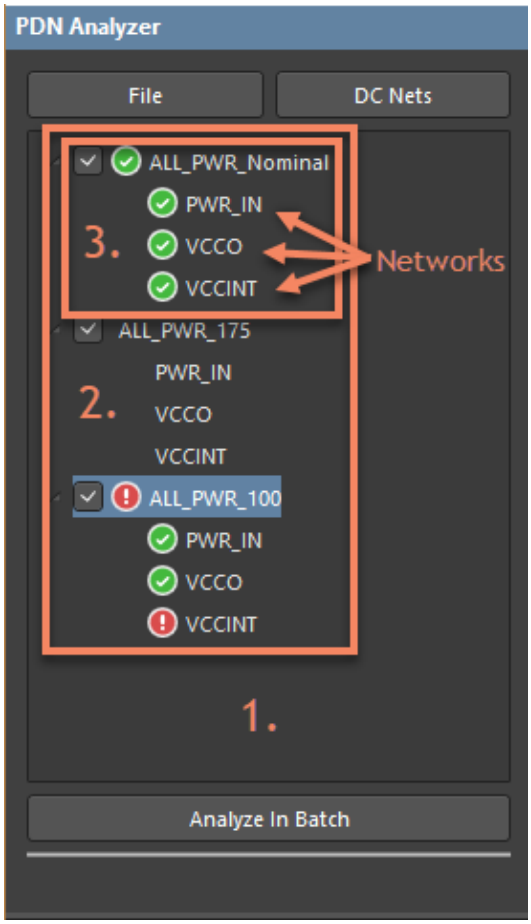
- Apply design information to ensure the most effective use of board space and easily identify, locate, correct, and report problematic high current density areas and voltage drop issues.

INTRODUCTION TO THE PDN ANALYZER INTERFACE

The **PDN Analyzer** extension interface is invoked as an **Altium Designer** non-modal panel, which can be positioned in any convenient location in the workspace or on another screen. The **PDN Analyzer GUI** is arranged with an upper section devoted to simulation/network control and an interactive representation of the currently selected power network(s), while the lower panel section provides access to the analysis options, display settings, and results data. Simultaneous multi-network simulation allows the direct current (**DC**) power integrity of an entire PCB design to be analyzed as a hierarchical structure or as individual power nets. The display and results configurations are available in the lower panel sections. Here are some definitions for important terminology used throughout the guide.

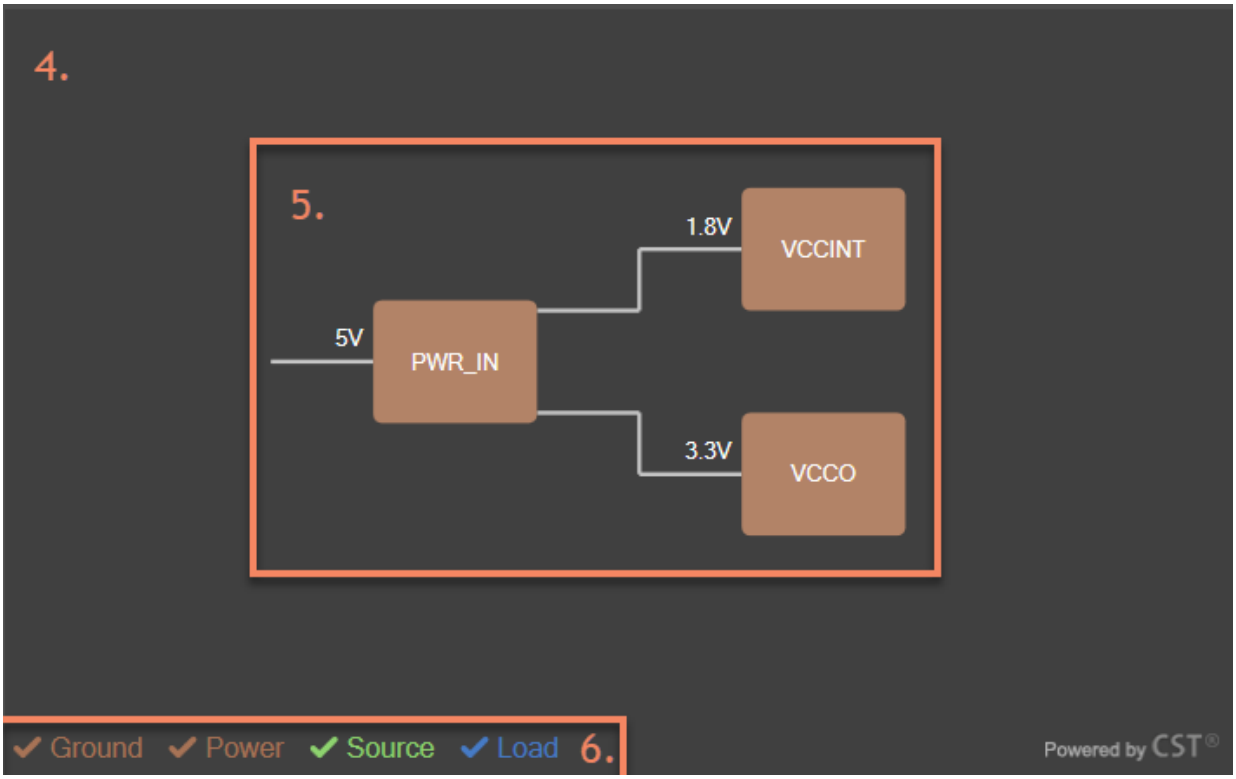
- **Net**: An electrical connection between two or more component pins in the design.
- **Source**: A component or circuit that provides power to the remainder of a defined circuit.
- **Load**: A component or circuit that requires power for operation.

- **Network**: This is a collection of power and ground **Nets**, at least one **Source** and at least one **Load**, arranged for the purpose of simulation.
- **Rail**: The collection of power nets or ground nets in a **Network** (e.g. a **Network Power Rail** or **Ground Rail**). The **Power Rail** is always rendered along the top of a Network, whether it is positive or negative in polarity.
- **Configuration** ("**config**"): A collection of one or more **Networks** to be simulated simultaneously.
  - **Config file**: A saved configuration with file extension "**.pdna**."
- **Simultaneous Multi-Network Simulation**: The co-simulation of all **Networks** in a **Configuration** including **Network** interactions. This happens automatically.
- **Batch Simulation**: The sequential **Simulation** of two or more **Configurations** in the **Simulation Tree**.



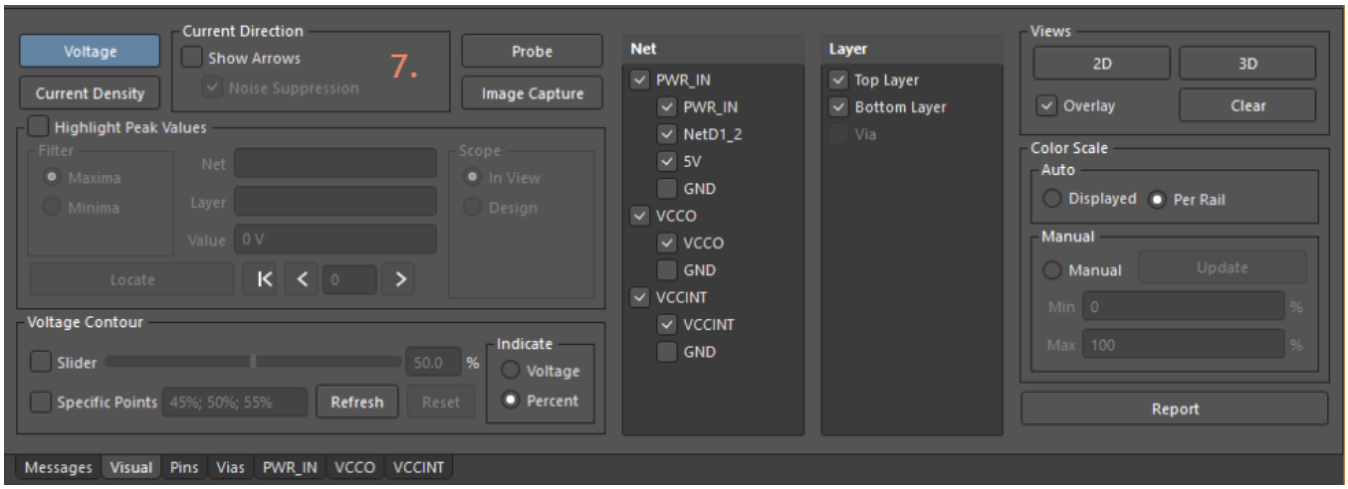
Simulation Pane

1. **Simulation Pane**: The upper left panel area used to manage **Network Configurations**.
2. **Simulation Tree**: The collection of **Configurations** in the **Simulation Pane**.
3. **Simulation**: A **Configuration** in the **Simulation Tree**.



Network Canvas

4. **Network Canvas**: The area in the upper-right of the PDNA panel.
5. **Block Diagram**: The auto-generated top-level view of a given **Configuration**.
6. **Simulation Readiness Indicators**: The color-coded legend in the lower-left portion of the **Network Canvas**.



Results Pane

7. **Results Pane**: The lower section of the PDNA panel.

The options outlined below provide a brief overview of the settings you will see on the **PDN Analyzer** interface. Resize the interface panel if some of these elements are not visible. Items with subdued background and muted text aren't yet editable – other information must be supplied before these are enabled for editing. Items that are bolder in shading and with clear text can be edited as necessary.

- **File** contains basic file operations and layout control.
  - **New Simulation** creates a new network simulation that can be configured as necessary.
  - **Open** allows loading **PDN Analyzer** configurations that have been previously saved.
  - **Save** allows saving **PDN Analyzer** configurations.
  - **Save As** allows saving **PDN Analyzer** configurations with a specific name.
  - **Explore** opens the Windows Explorer project source file location.
  - **Explore Samples** opens the windows explorer file location
  - **Compact Layout** modifies the panel layout to facilitate docking.
- **DC Nets** opens the **PDN Analyzer DC Net Identification** dialog.
- **Analyze** at the bottom left is only enabled once all required parameters are provided.

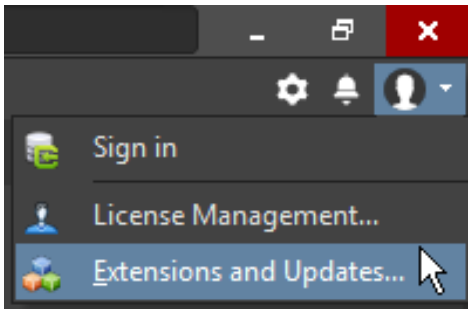
INSTALLATION AND LICENSING

The **PDN Analyzer** application is added to **Altium Designer** by installing the **PDN Analyzer Extension**. Its functionality is enabled with a matching software License.

Installation

PDN Analyzer is installed and updated from the **Extensions & Updates** view.

1. Select the **User** drop down menu located at the top right of the **Altium Designer GUI**.



Extensions and Updates View

2. Select the **Extensions & Updates...** view.
3. Select the **Purchased** tab.

4. Locate the **PDN Analyzer icon** and then click its  button to download and install the extension.

PDN Analyzer Icon

5. Click **No** when asked to create a trial license.
6. Restart **Altium Designer** to enable the application.

A timed **Trial License** may be offered for **PDN Analyzer**. If you wish to use **PDNA** on a evaluation basis, follow through the guided steps and confirm the license activation in the **License Management** view. Otherwise, proceed with a standard license scheme as described below.

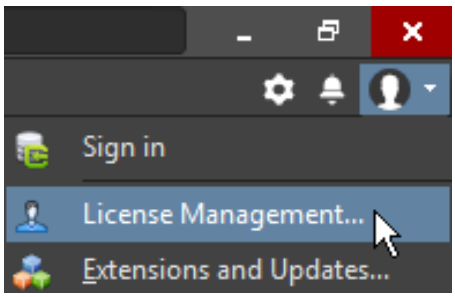
Once installed, the extension will appear under the **Extension & Updates** view's **Installed** tab. When a **Schematic** or **PCB** project document is open, **PDN Analyzer** is available from the **Altium Designer Tools** menu as **PDN Analyzer**. Note that if **PDN Analyzer** is unlicensed, a related error message will appear.

Licensing

PDN Analyzer can be licensed using any of standard **Altium License** schemes:

- On-demand
- Standalone license
- Internal network Private License Server

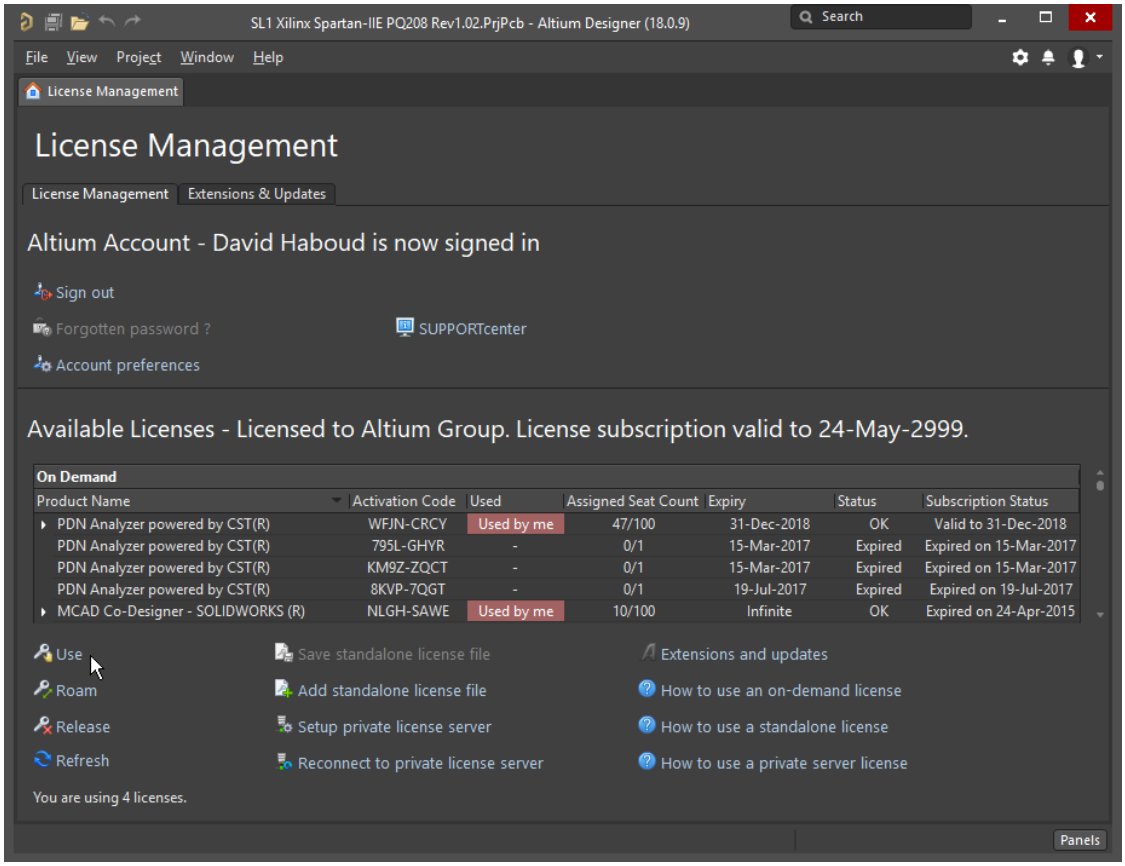
1. Select the **User** drop down menu located at the top right of the **Altium Designer GUI**.



License Management View

2. Select the **License Management...** view.
3. Scan through the **Available Licenses** list for a **PDN Analyzer powered by CST®** license entry.
4. Select the desired **license type**.

5. Click the **Use** link to activate your **PDN Analyzer** license.



License Management

When the license is activated, its **Assigned Seat Count** number will increment and the entry's **Used** column will include a '**Used by me**' entry.

– See the **Altium Designer Licensing** page for more information on Altium licensing and types of licenses.

Once installed and licensed, the **PDN Analyzer** icon will also appear under the **Updates** tab (in **Extensions & Updates...**) when a new version is available for download. Hover the mouse cursor over the icon's download button to see the version information, or select the extension's title to expose more information.

– See the **Altium Designer Extensions** page for more detailed information about installing and managing extensions.

PRACTICAL EXAMPLES AND DEMONSTRATIONS

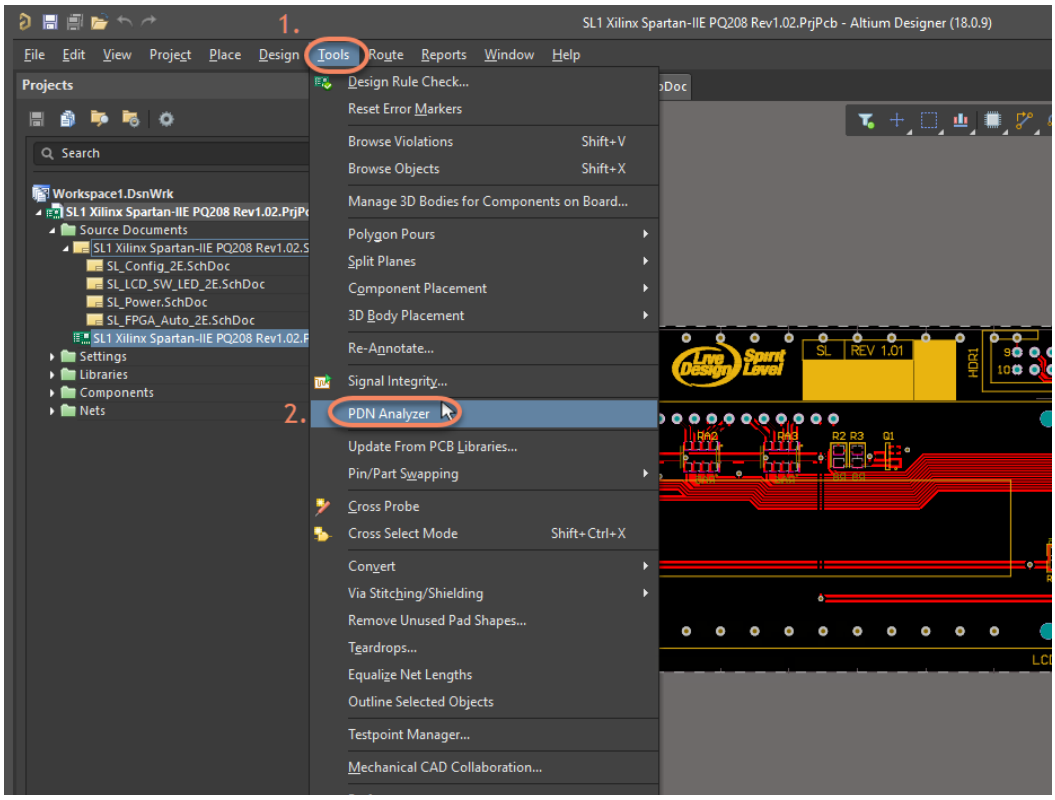
We will be using the **SpiritLevel-SL1** design for the three examples in this guide. By default, these files can found in the example folder of your **Altium Designer** installation folder: **C:\Users\Public\Documents\Altium\ADxx\Examples\SpiritLevel-SL1**

You can download a zipped copy of the files under **File >> Explore Samples**.

Pre-simulation DC Net Identification

When **PDN Analyzer** is initially opened for a PCB design, it will attempt to identify all DC power networks from the design's net data based on common power network nomenclature. Proper DC net identification is important to gain the most accurate simulation results. The primary DC nets have already been identified in the example project to streamline the process.

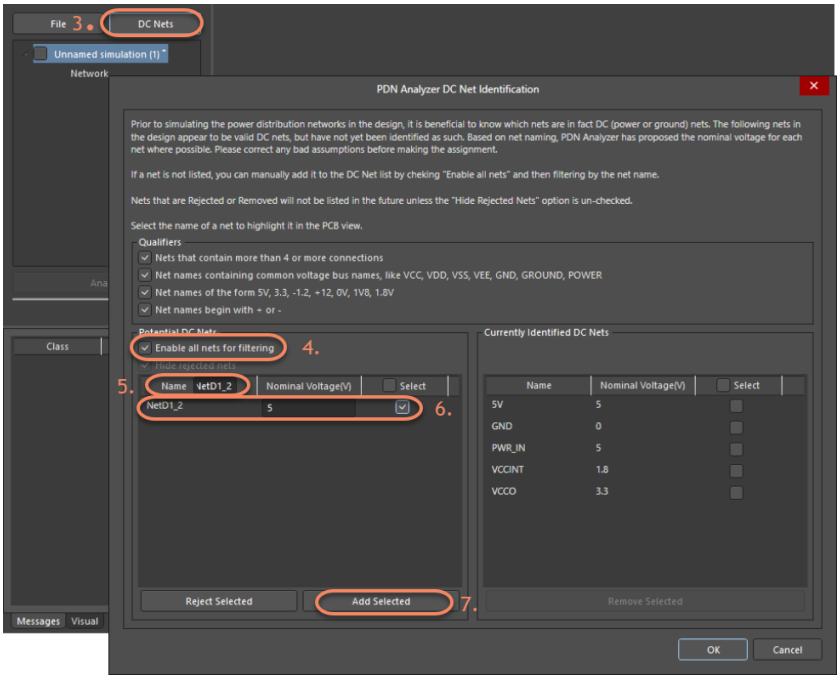
1. Open the PCB document from the **SpiritLevel-SL1** project.
2. Select the application from **Tools » PDN Analyzer**.



Opening **PDN Analyzer**

3. Click **DC Nets** for opening dialog **PDN Analyzer DC Net Identification**.

Note: This dialog will open automatically after first start of **PDN Analyzer** with a new design with undefined **DC Nets**.



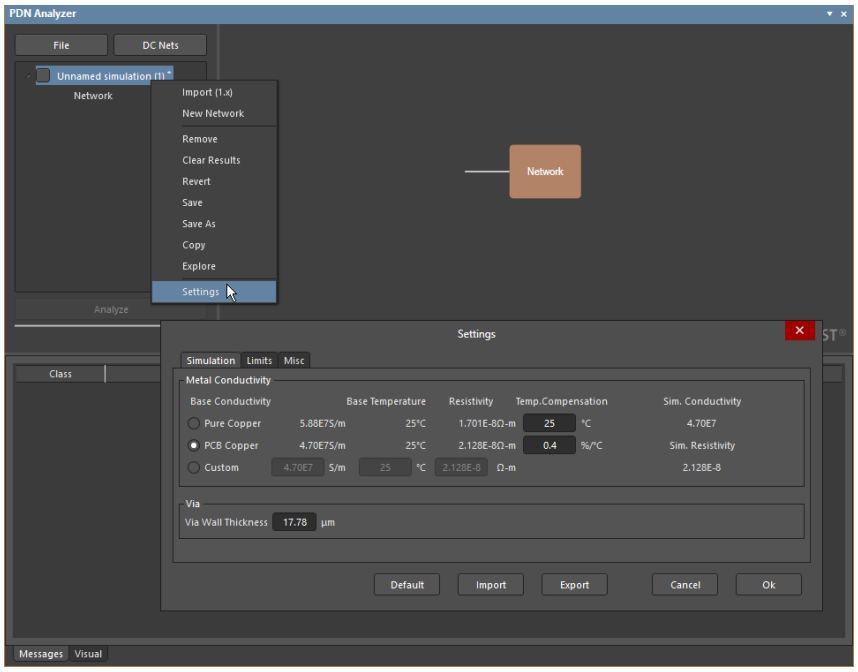
PDN Analyzer DC Net Identification

4. Select the **Enable all nets for filtering** option to ensure all potential power nets have not been identified.
5. Type **NetD1_2** in the header search filter.
6. Select the **NetD1_2** checkbox to add to the preconfigured power nets available for PDN analysis.
7. Set the **Nominal Voltage** fields to 5V for **NetD1_2** .
8. Click the **Add Selected** button to populate the **Currently Identified DC Nets** list.
9. Confirm these nets as identified power networks by clicking **OK**.

Note: Click on a listed net entry in the dialog will cross probe to that net in the PCB layout. Further nets can be identified and applied at any time by selecting the **DC Nets** button in the main panel interface.

Simulation Settings

10. The results from an analysis, and in particular the degree of IR losses in the board shapes, will also depend on the specification for the board *copper conductivity* and *via wall thickness*. Any changes to the simulation settings require analysis to be rerun to take effect. Refer to altium.com/documentation for more information about **Simulation** settings.
11. Right-click on the current analysis setup name and select **Settings** from the context menu.



PDNA Settings

Metal Conductivity Definition

The **Metal Conductivity** section of the dialog provides details and settings for the *conductivity* value (the ability of your metal to conduct electrical current and the inverse of *resistivity*; 1/R) of the metal used in a design. The **base conductivity**, **resistivity**, **base temperature**, **temperature compensation** (simulation temperature), and/or **resistivity thermal coefficient** (the percentage increase in resistivity per degree Celsius) can be selected or modified in the dialog to reflect a design's board construction properties:

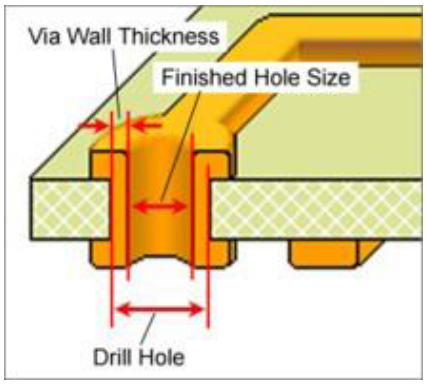
Note: The displayed **Sim Conductivity** figure represents the final conductivity value after taking into account all temperature compensation parameters relating to the defined **Base Conductivity**. The **Sim Resistivity** represents the inverse of **Sim Conductivity**.

Via Wall Definition

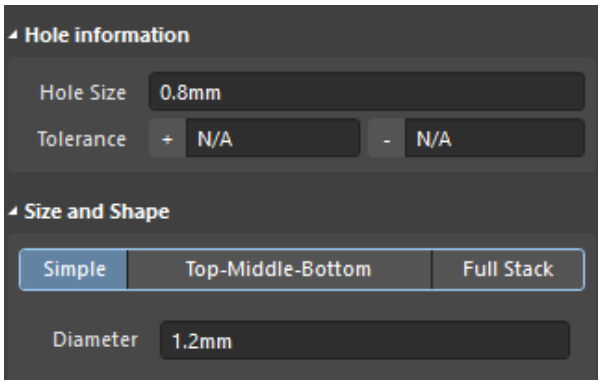
The **Via Wall Thickness** value specifies the thickness of the **Via Wall (plated through-hole) Metal** for all vias in the design simulation analysis. The setting can noticeably affect the power network DC losses due to the inherent resistance a ***thin-walled (plated)*** via represents. When of sufficient in quantity, **size and thickness** however, a via (or vias) will not impede a design's DC performance, and will exhibit similar current density as the power traces it connects – and negligible voltage loss between its connection points.

In terms of the simulation, the via size and wall thickness effectively defines the amount of conductive material represented by the via, and therefore its resistance/conductivity. The simulation assumes that the via diameter represents the finished hole size and the via wall thickness then increases the via diameter. Therefore:

Finished Hole Size = Hole Size - (2x Via Wall Thickness)



Via Dimensions



Altium Designer Via Dimensions

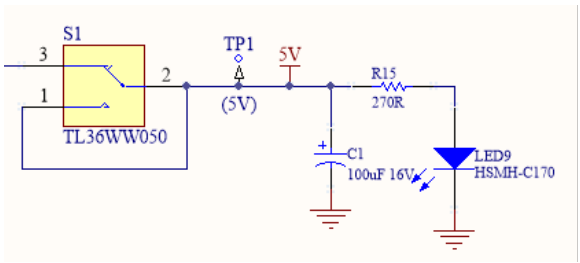
Limits Settings

Defining specific current and current density limitations will trigger a violation when exceeded. Current density limits for surface/internal layers and vias are specified under the **Limits** tab in the **Settings** dialog. The specified current density limitations will apply automatically to a completed analysis. Any networks that contain violations are shown with a dashed red outline.

You can determine a current limits from defined trace widths and vias with formulas from IPC-2221. **PDN Analyzer** maps appropriate current limits for all via hole sizes ranging from defined **Hole Size 1** to **Hole Size 2**. There are no default limits set to a new design analysis. Current limitations have been placed on vias to demonstrate functionality in Example 3.

EXAMPLE 1 - SIMPLE 5V SUPPLY RAIL DISTRIBUTION

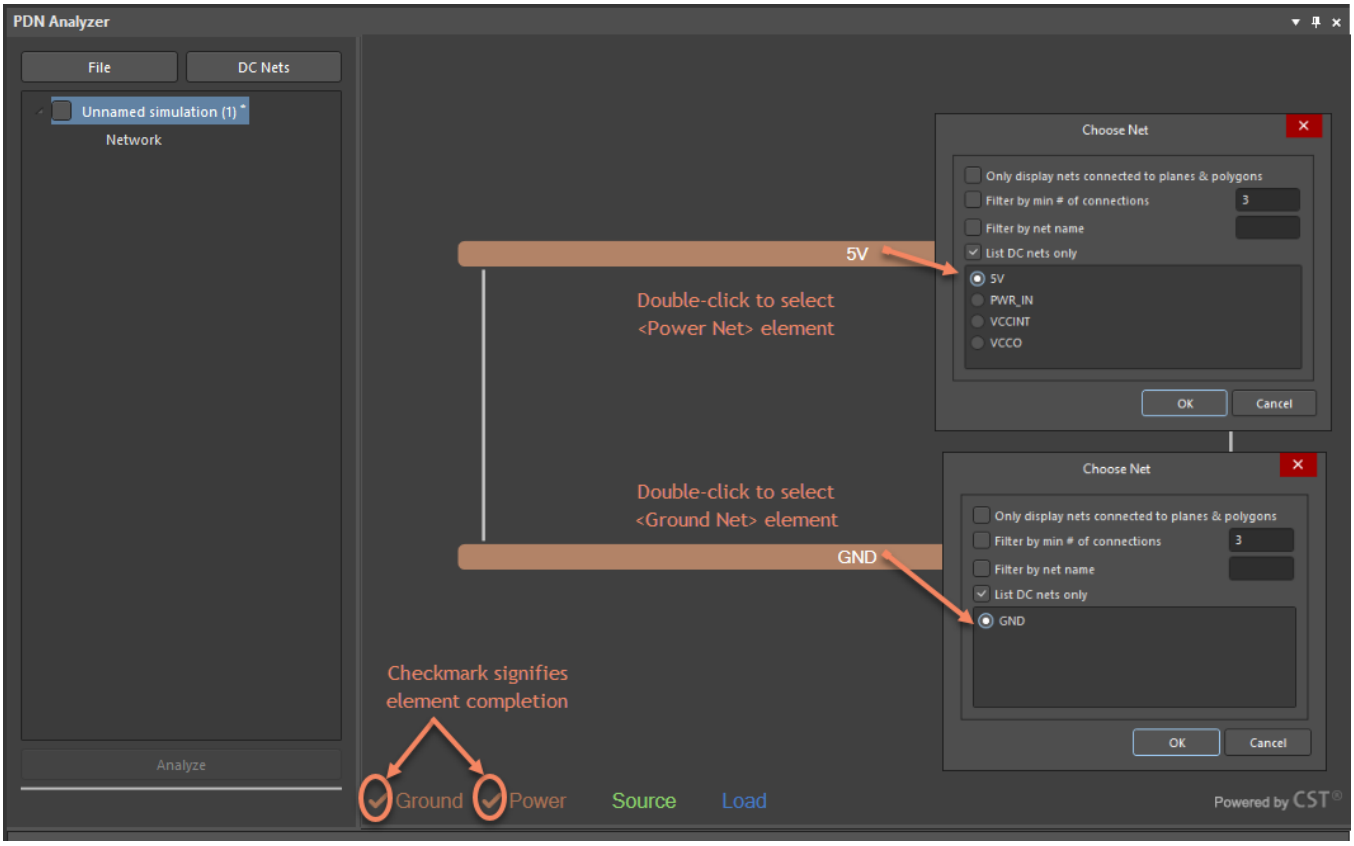
This example demonstrates the basics of setting up a power integrity simulation with a simple power net and its current loads. It is configured to assess the **5V** supply rail distribution and its ground return path in the **SpiritLevel-SL1** reference project, when loaded with the design's LCD display. In this case, the **5V** supply rail is considered as a simple voltage source, and its connected networks (such as via switch **S1**) are not included.



5V Supply Rail

DC Network Setup

1. Double-click on the **Network** element in the **SImulation Pane**.
2. Double-click on the **<Power Net>** element in the **Network Canvas** (see picture below) to open the Choose Net dialog (only identified **DC** nets are shown by default).



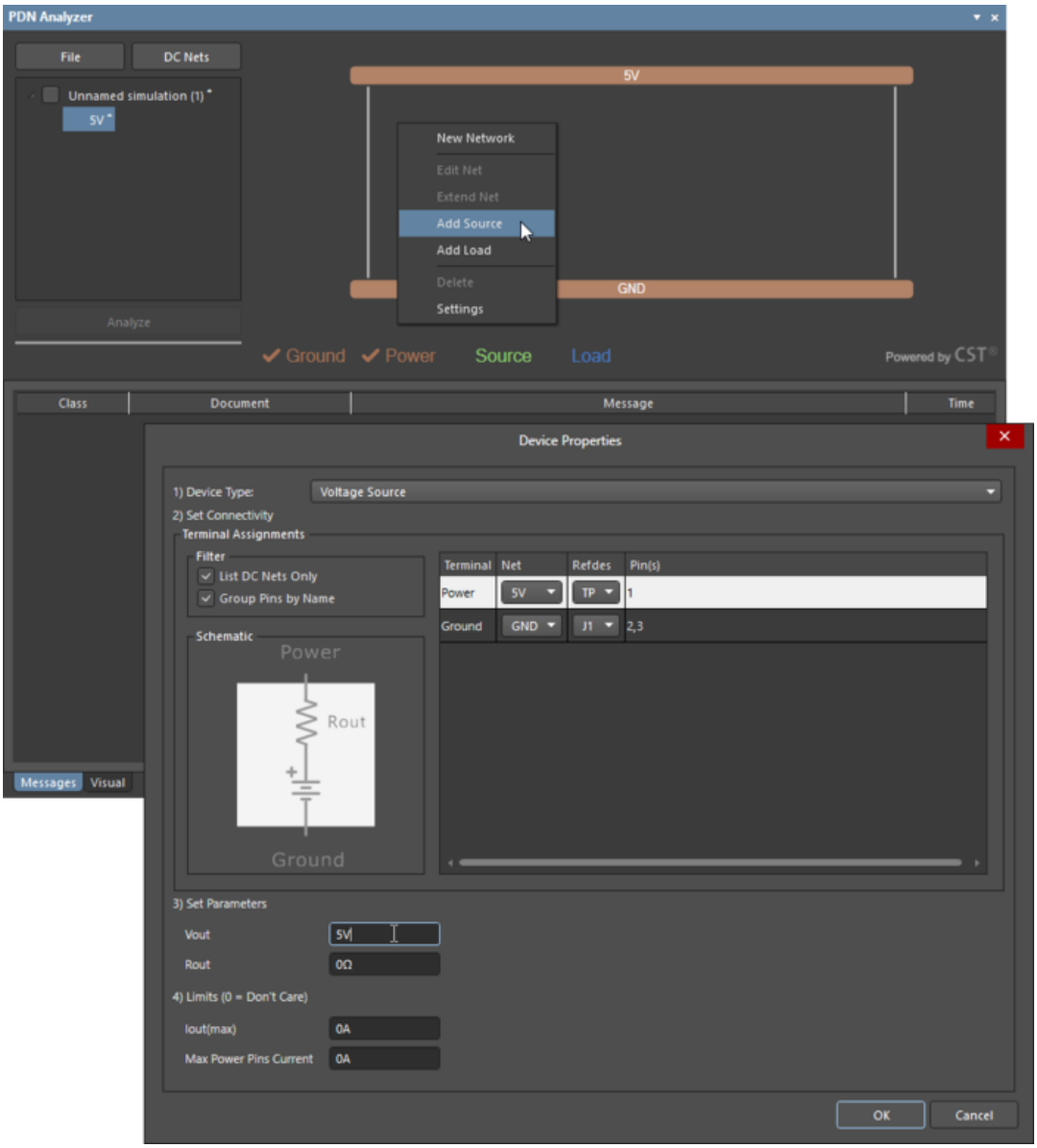
DC Network Setup

3. Select **5V** and click **OK**.
4. Double-click <**Ground Net**>.
5. Select **GND** and click **OK**.

Note: The Ground and Power **Simulation Readiness Indicators** are now checked (✓).

6. Add a **Source** element by right-clicking in the network graphic workspace and select **Add Source** from the context menu to open the **Device Properties** dialog.
7. Select the **Voltage Source** option from the dialog's **Device Type** drop down menu.
8. In the source connectivity listing, PDNA will attempt to choose the correct net connection options based on the power network parameters – this is between the 5V and GND nets.
9. Use the **Refdes** drop down menu options to specify the component connection points of the **source voltage** as **TP1** and **ground** return **J1** (pin **2** and pin **3**).

10. In the lower section of the dialog, set the **source voltage** (**Vout**) to **5V** and the model's internal resistance (**Rout**) to **0Ω**.
11. Click **OK**.



Setting Voltage Source Properties

11. Add a **Load** element by right-clicking in the network graphic workspace and select **Add Load** from the context menu to open the **Device Properties** dialog.
12. Set **Device Type** to **IC (Current)** to represent the current drawn from the 5V rail by the LCD component.

Note: A purely resistive load option is also available, by choosing **Resistor** as the **Device Type**.

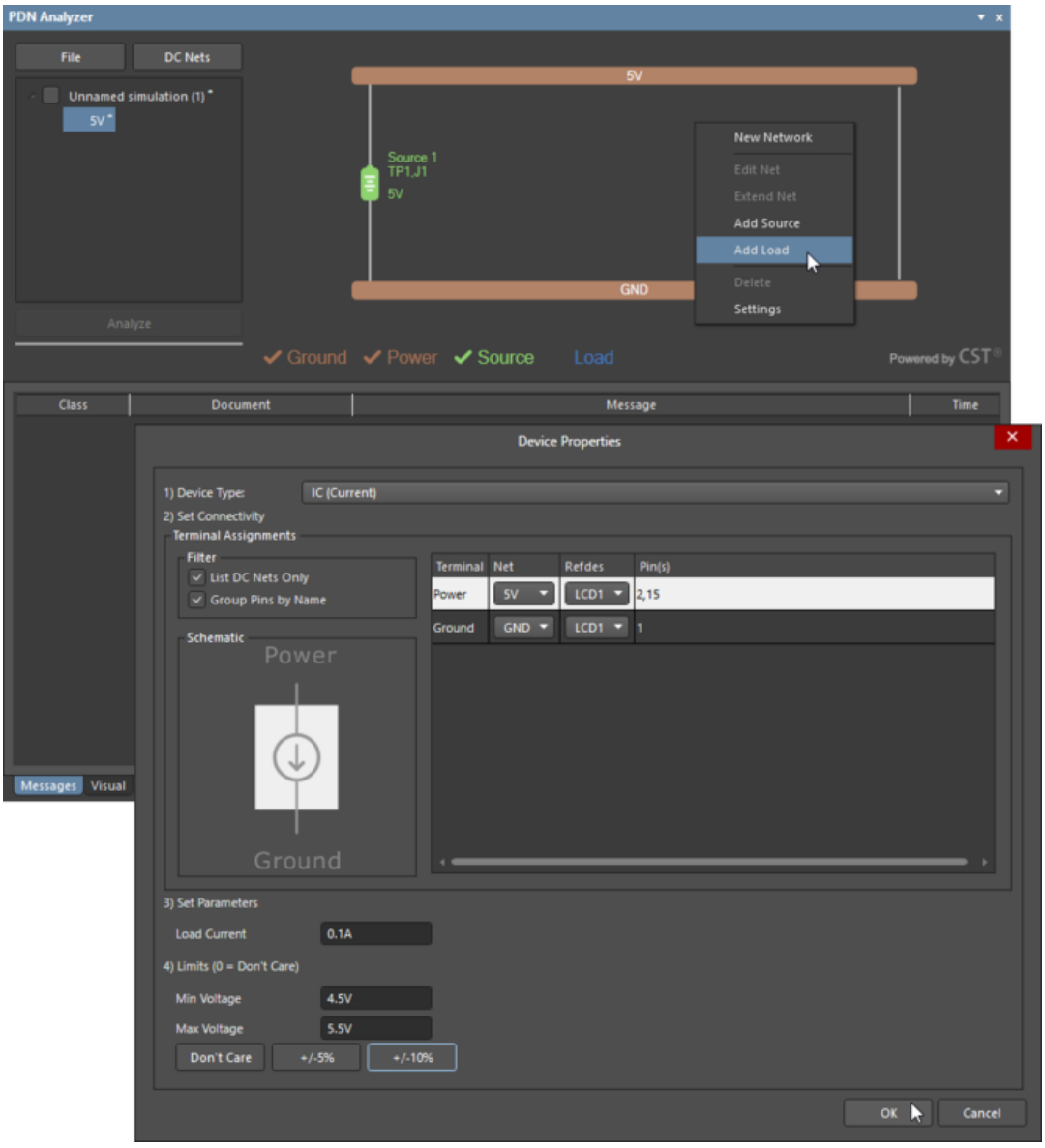
13. Use the **Refdes** drop down menu options to set the load connection as **LCD1** and set **Load Current** to **0.1A**

Note: Unit prefixes are interpreted by the system, for example, 500m resolves to 0.5A.

14. While the voltage **Limits** settings are optional, set **Limits** by pressing the **+/-10%** button. This will trigger a simulation violation if the voltage at the load itself drops below **4.5V** or above **5.5V** in this simulation.

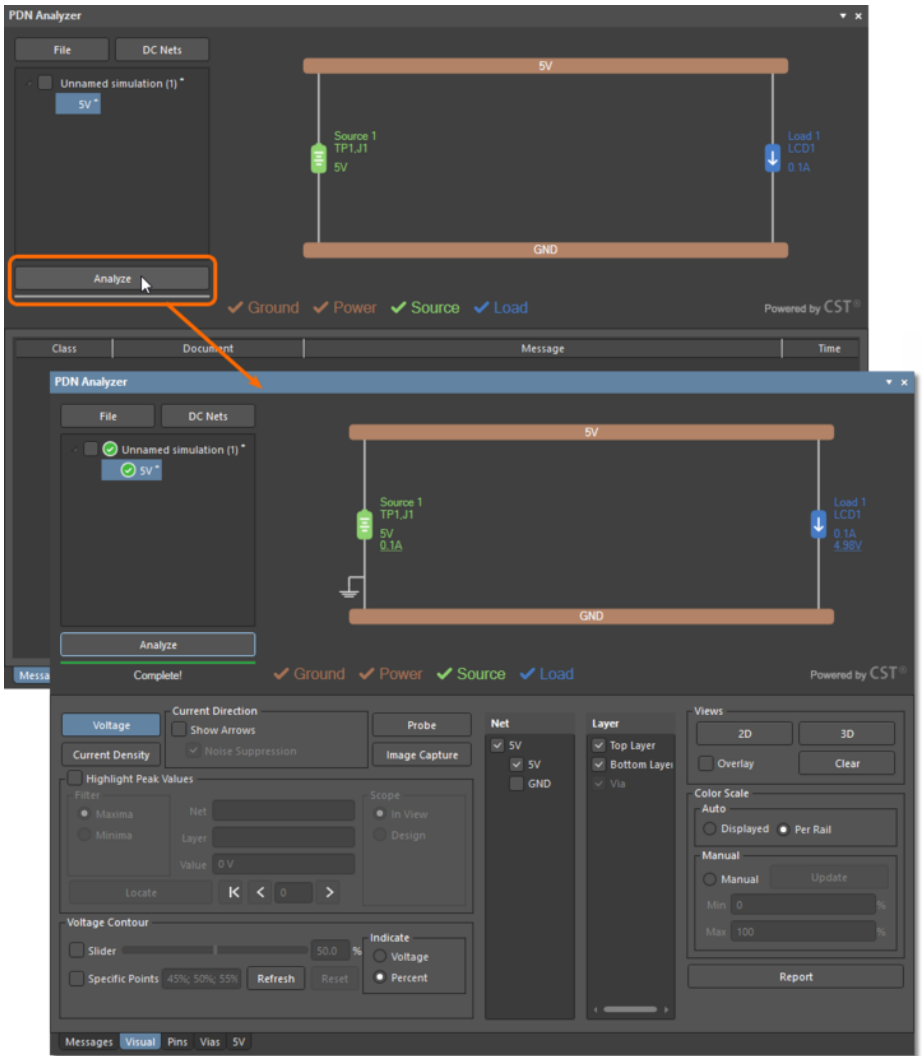
15. Click **OK**.

Note: With the power network defined and all parameters specified all network elements should have an associated ✓ status.



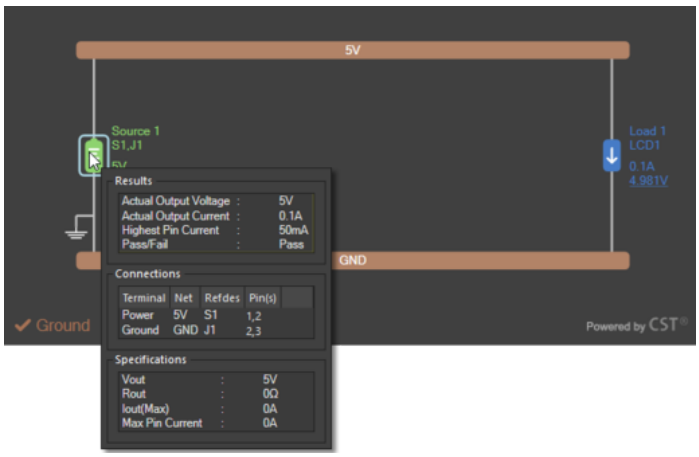
Setting Load Properties

17. Select the Analyze button.



Initiating Analysis

The progress of the simulation is shown under the **Messages** tab as a stream of events, which will also indicate the cause of a simulation failure if the process is unable to complete. The immediate results of the PDN analysis can be seen in the network graphic, which will include the calculated load/source voltage and current levels (where applicable), and the highlighting of any sections of the network that have caused a parameter **Violation**. The **Visual** tab becomes focused and active upon simulation completion. Hover the cursor over any element in the network (**Load**, **Source**, or **Series Element**) to see additional information such as its specified parameters and analysis results.

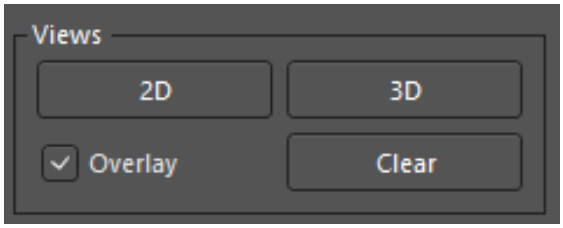


Addition Source Information

VISUAL POWER ANALYSIS AT DESIGN TIME

The results of simulation can be viewed graphically in the Altium Designer PCB editor controlled by the **PDNA Visual** tab. The view of the selected net path voltage drop, in this case from the **5V** source at **TP1** to the **LCD1** component, is rendered with a color gradient that corresponds to the **Voltage** scale presented at the bottom of the view. This is shown as a voltage percentage (the **Per Rail** option under **Color Scale**), or as a literal voltage span (the **Displayed** option).

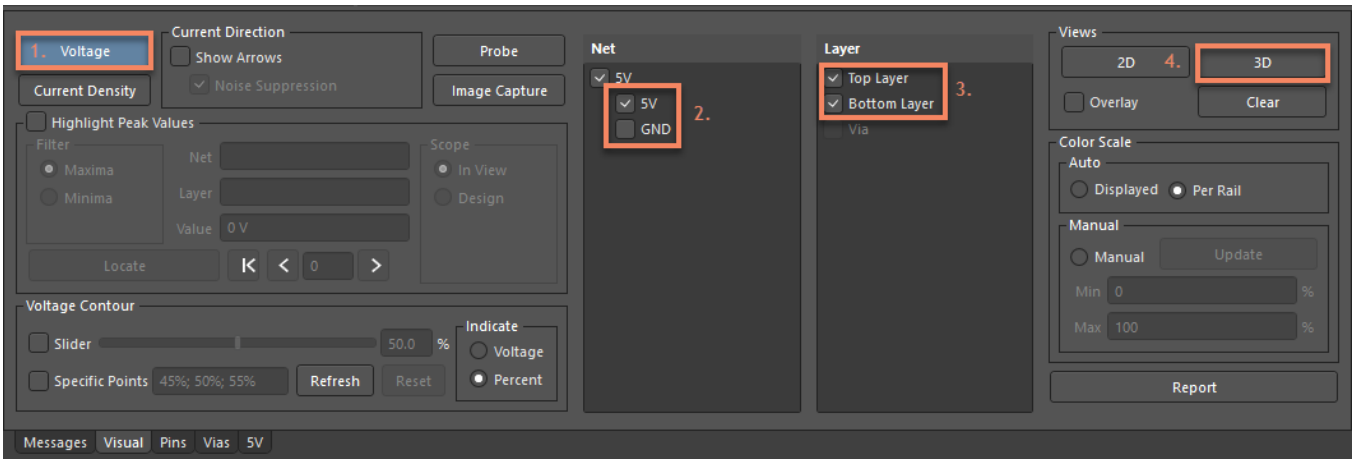
PDN Analyzer offers several interactive display options that determine how the analysis results are graphically represented in the Altium Designer PCB Editor. Along with the options for the display **Color Scale**, the graphics can be switched between **2D** and **3D** rendering, where the latter provides a valuable insight into the analysis results through vias and between layers that cannot be seen in **2D**. We will explore specialized features in **Example 3**.



Visual Tab Views Section

Voltage Drop View

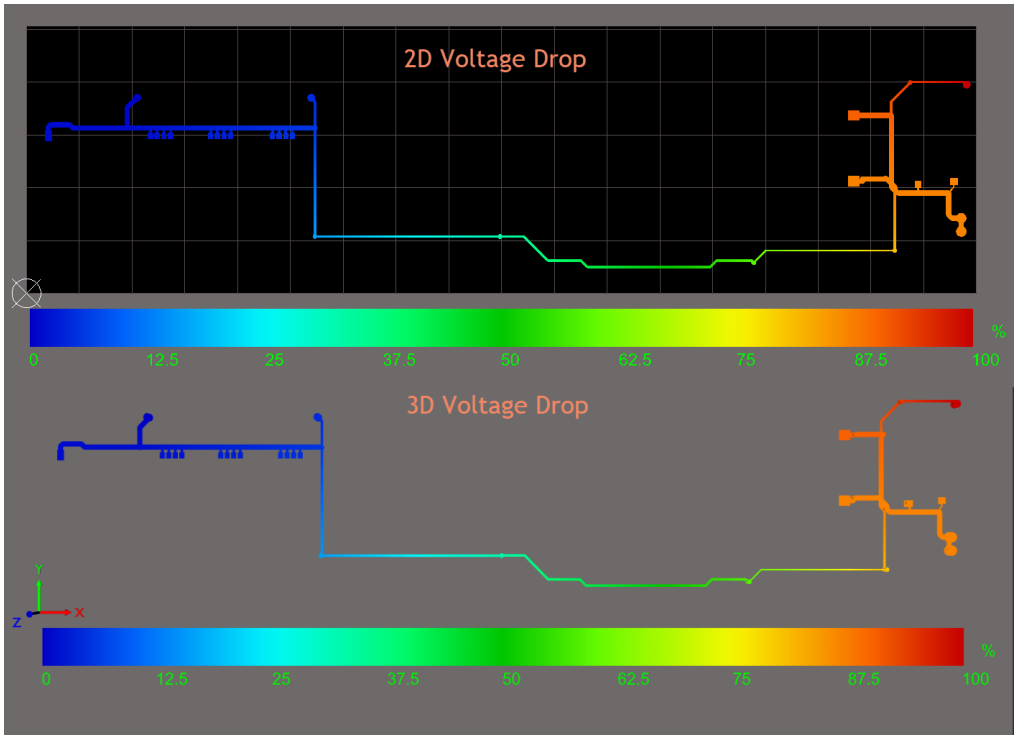
1. Select the **Voltage** option in the **Visual** tab.



Enabling Voltage Drop Results

2. Enable the **5V Net** visual options to display **Voltage Drop** across the network.
3. Enable the **Top** and **Bottom Layers**.
4. Click the **3D** button in the **Views** section.

Note: This option is particularly useful for confirming where a point of interest in the analysis results is located in the board layout itself.

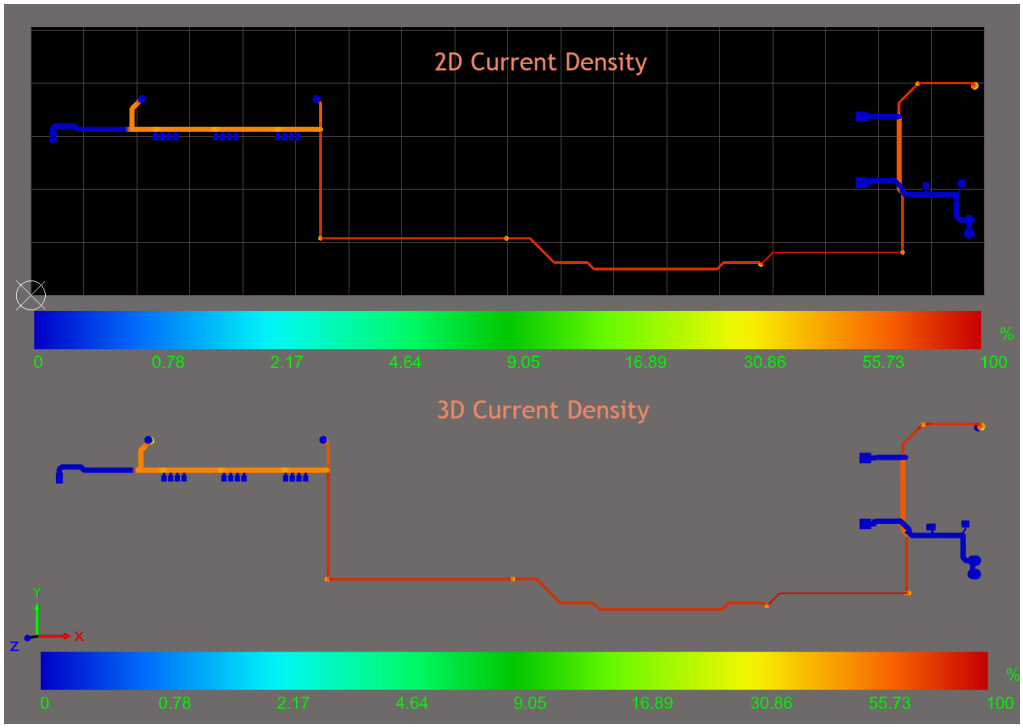


2D and 3D Voltage Drop

5. Clear the analysis results from the editor display with the **Clear** button in the **Views** section of the **Visual** tab.

Current Density View

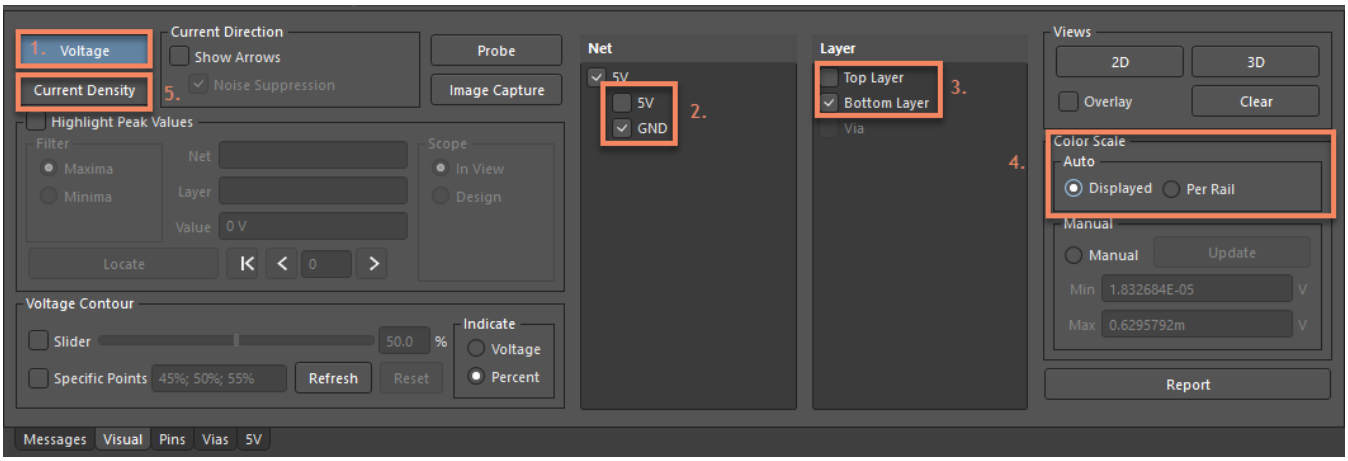
1. Select the **Current Density** option in the **Visual** tab.
2. Click the **2D** button in the **Views** section.



Current Density in Results View

Visual Analysis of the Return Path

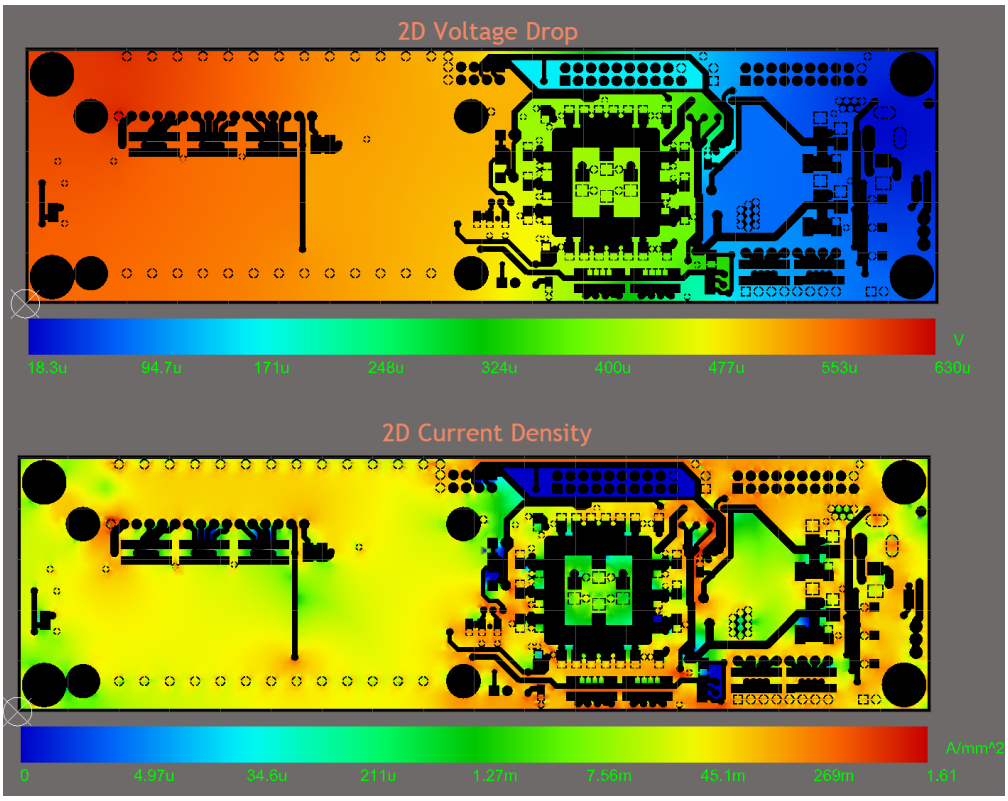
1. Select the **Voltage** option in the **Visual** tab.



Setting Up Return Path Analysis

2. Deselect the **5V** network option in the **Net** list under the **PDNA Visual** tab and select the **GND** network.
3. Enable only the **Bottom Layer** of the **GND Net**.
4. Set the **Color Scale** to **Displayed**.
5. Switch to **Current Density** view.

Note: Maximum current "**hotspots**" are easy to identify in red.

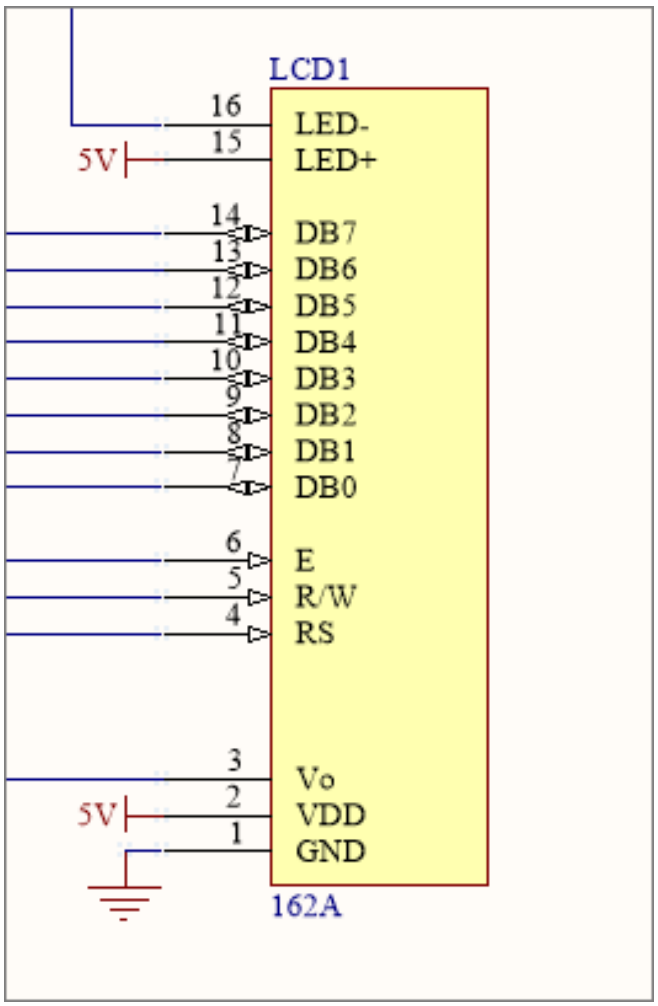


Return Path Analysis Results

Representing Complex Load Models

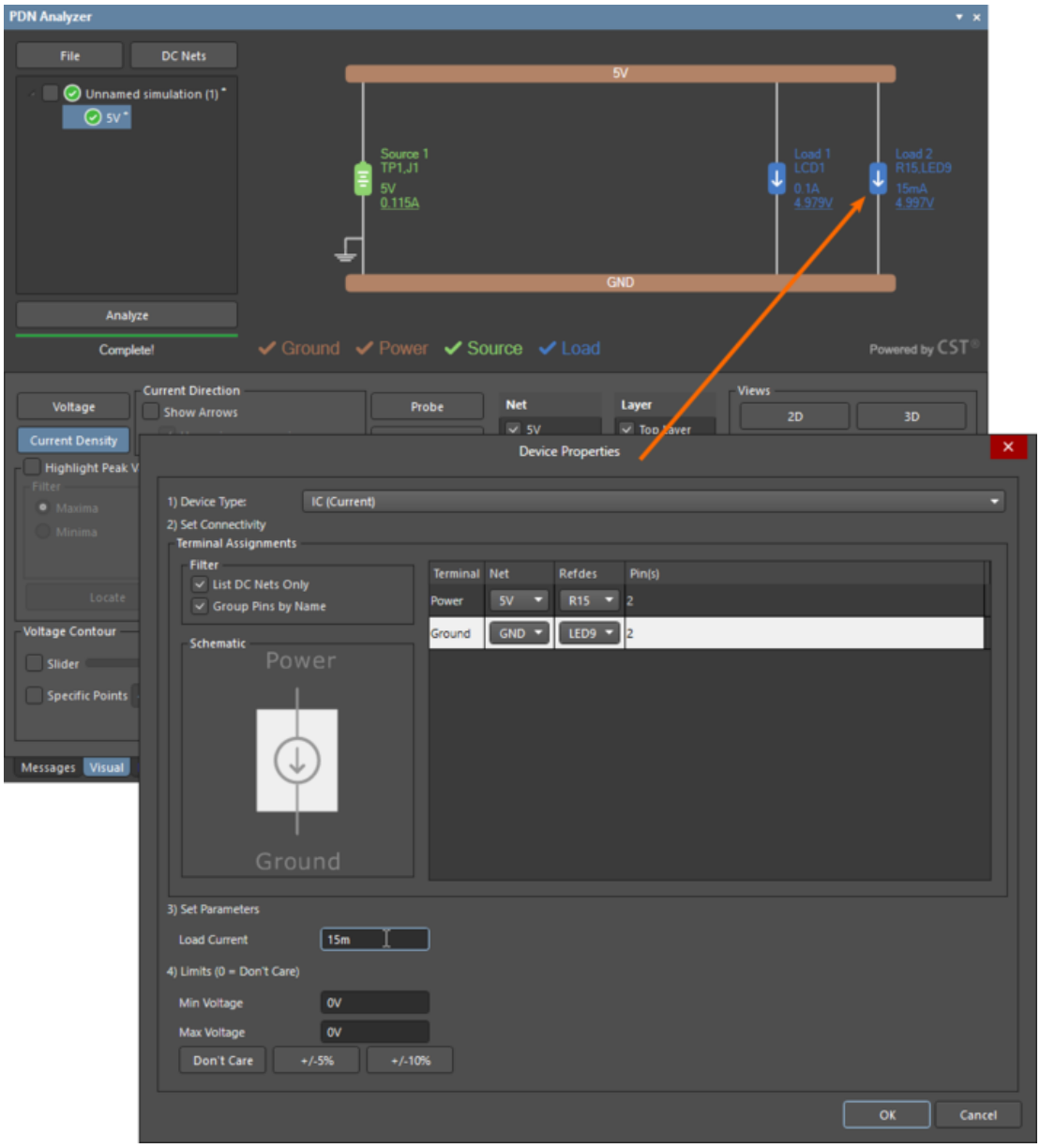
Further loads can be added to the network as required and the power analysis re-run to assess the results. For example, you can add the small load current (**15mA**) attributable to the design's power LED and re-run analysis. PDN Analyzer allows device pin connection definitions for a load. Defining pin connections allows the creation of multiple load models for a single component device with different current consumption across pins.

The LCD device in the example project demonstrates this situation, where its **5V** connection at **pin 15** (**LED+**) powers the display backlight, while the **5V** connection at **pin 2** (**VDD**) powers the internal logic – in practice, **pin 15** will consume significantly more current than **pin 2**. Representing **LCD1** as two load models improves the accuracy of the power analysis: one for each **5V** pin and its associated load current. When added as a single PDNA load model, both pins for **LCD1** are nominated (by default) as the 5V load connection, and the PDN analysis distributes the **LCD1** load current equally between these pins.



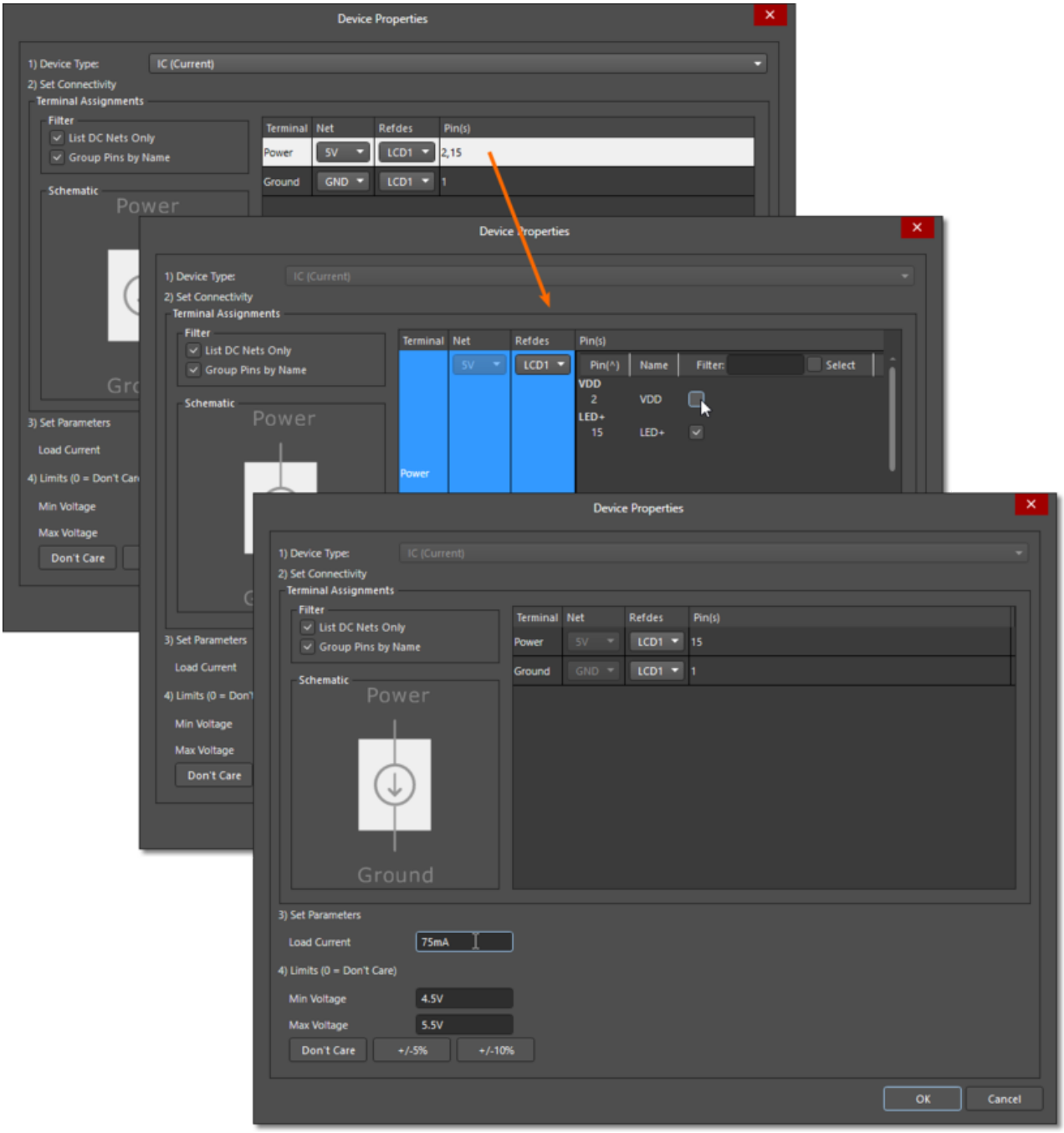
LCD1 Schematic Symbol

1. Return to the analysis setup and **Add Load**.
2. Select the series resistor (**R15**) as the **5V** rail connection and the LED pin (**LED9**) as the **GND** connection.
3. Click **OK**.



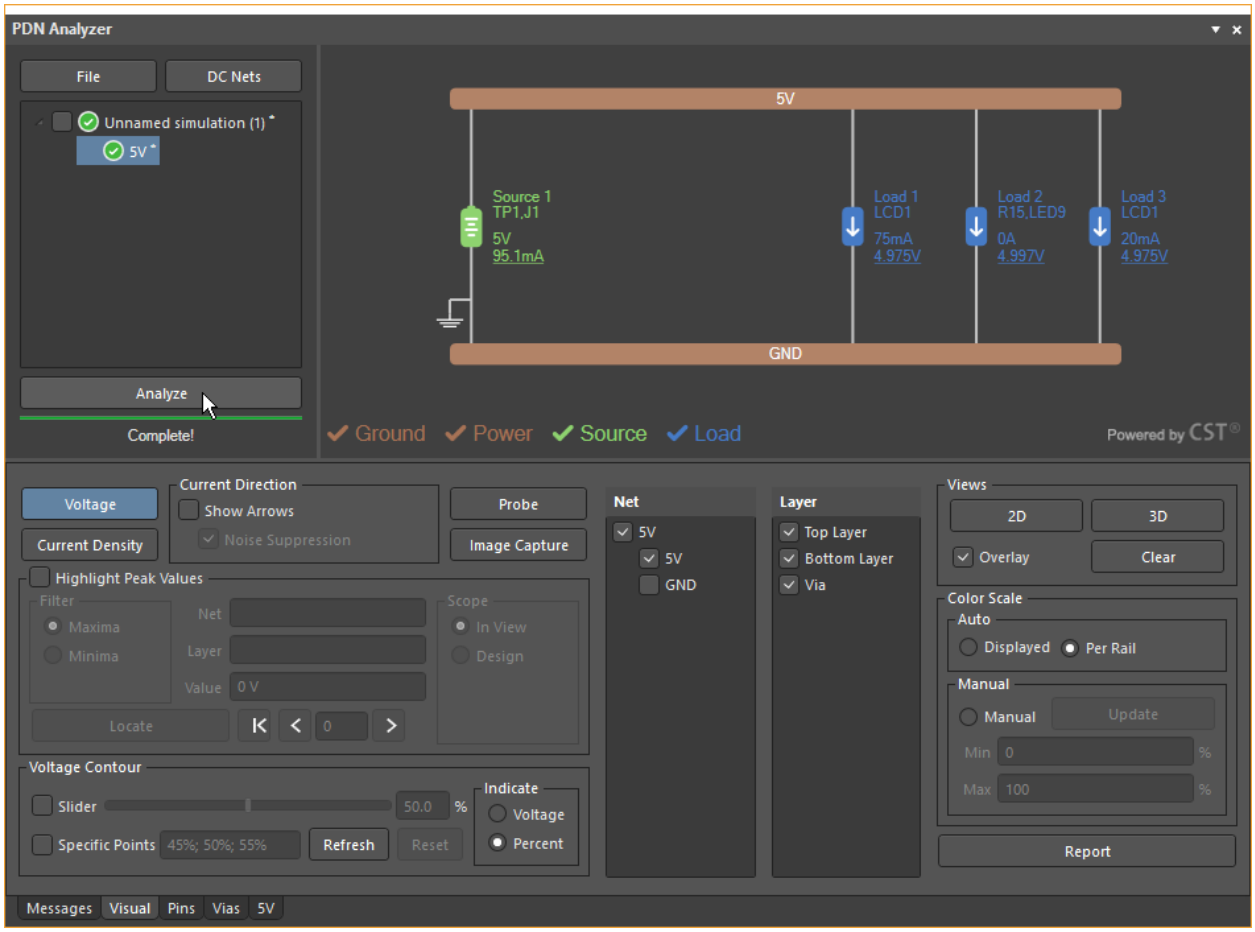
Adding a Load to an Existing Network

1. Return to the existing **Network Setup** and **double-click** on **Load 1**, **LCD1**.
2. Double-click on the **Power** net **Pin(s)** parameters of the existing **LCD1** load model.
3. Deselect the **VDD** (**Pin 2**) checkbox.
4. Set **Load Current** to **75mA**.
5. Click **OK**.

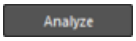


LCD LED Load Model

6. Add another load for **LCD1 Pin 2**.
7. Use the **Refdes** drop down menu options to set the load connection as **LCD1** for the **Power** and **GND** nets.
8. Double-click on the **Power** net **Pin(s)** parameters of the existing **LCD1** load model.
9. Deselect the **LED**+ (Pin 15) checkbox.
10. Set **Load Current** to **20mA**.
11. Set **Limits** by pressing the **+/-10%** button.
12. Click **OK**.

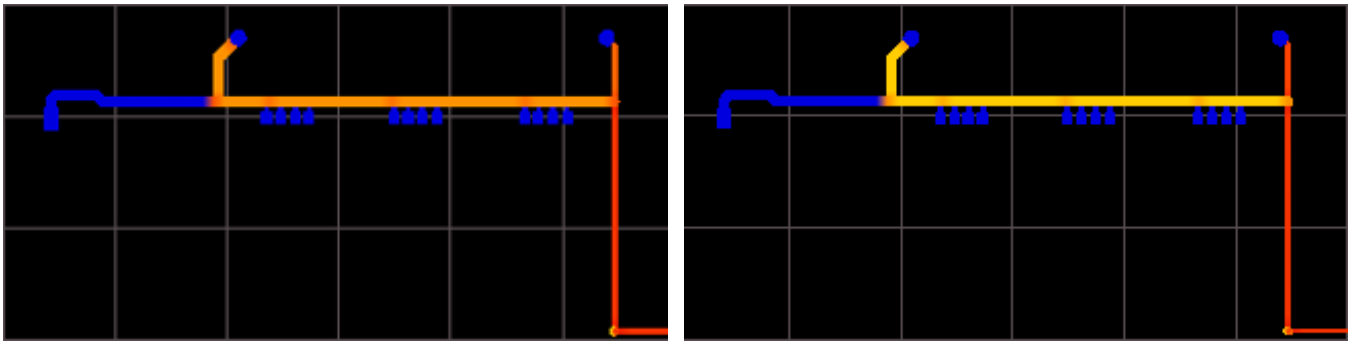


LCD1 Represented with Two Load Models

13. Click  .

The difference in load current distribution can be seen when comparing the **Current Density** of the **LCD1** power network tracks between the original and updated load arrangements. The below **Current Density** analysis images show the original, single load **LCD1** model result on the left, and the updated multi-load result on the right.

Note the current density in the tracks supplying **pin 2** (the **LCD** pad towards the left) and **pin 15**. The updated version correctly shows the majority of **LCD** current flowing to **pin 15** (the LCD pad towards the right), rather than being evenly distributed between the two pins, as was the case (left image).

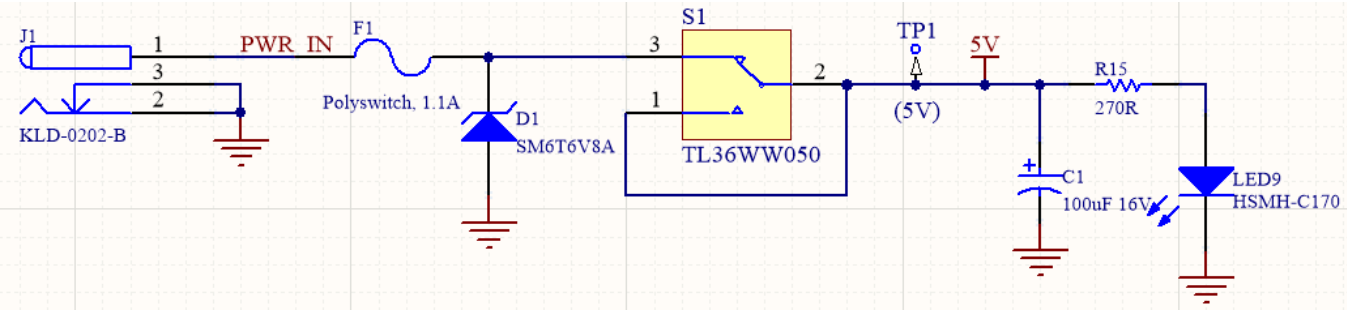


LCD1 Single Vs. Multi-Model Load Analysis Comparison

EXAMPLE 2 - SERIES POWER NET CONNECTIONS

This example demonstrates how to implement a series of connected nets that can be analyzed as a whole, while taking into account the parameters of the series elements that interconnect them. It also provides an overview of adding **Voltage Regulator Models** (**VRMs**) elements, which also act as electrical and logical links between networks, and how a complete hierarchy of a design's power network is developed.

The example models the **PWR_IN** to **5V** network of the SpiritLevel-SL1 reference project, and includes both the **3.3V** (**VCCO**) and **1.8V** (**VCCINT**) **VRMs** to create a complete power network structure.



Schematic Power Network

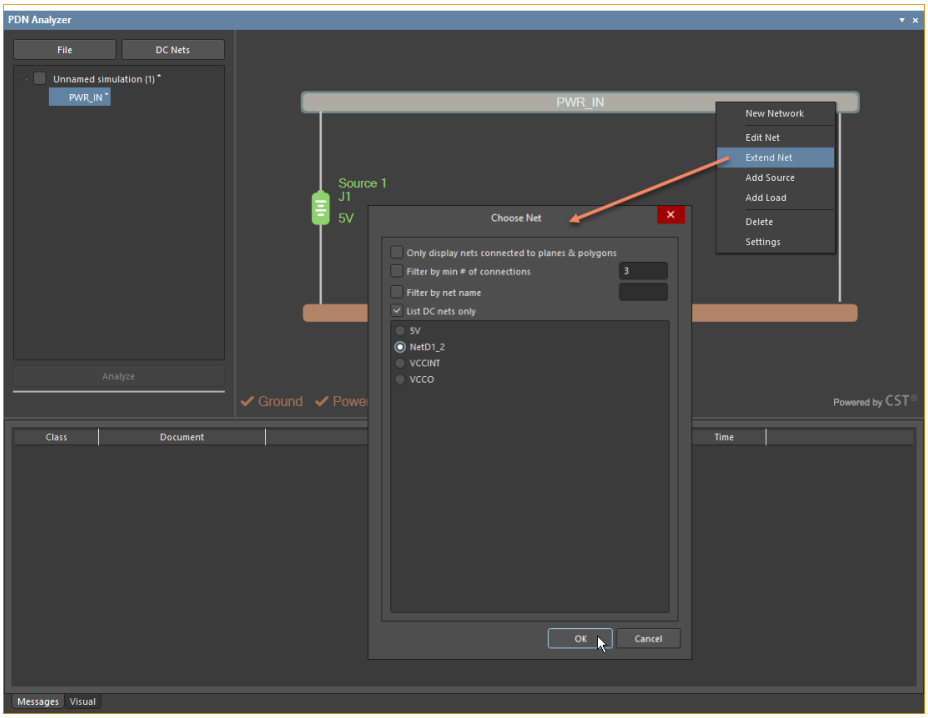
DC Network Setup

1. Select **File » New Simulation**.
2. Set the **<Power Net>** to **PWR_IN** and **<Ground Net>** to **GND**.
3. Add **Source** and set to **J1**.

Extending Networks through Series Elements

Modeling the full power path from the **PWR_IN** network to **5V** network, the series fuse (**F1**) and switch (**S1**) components along with their intervening net need to be added. In the PDNA interface, these are added by sequentially extending the power network. Each net "**extension**" is connected by a universal series element model. A series element is not restricted to a single RefDes for all terminals. For example, a series element can be made to model an inductor or it can span multiple components in case a portion of the design does not need to be simulated or because power leaves the PCB on one connector and re-enters on another.

1. Right-click on the **PWR_IN** network and select the **Extend Network** option from the context menu.
2. Select the **NetD1_2** net (bridges **F1** and **pin 3** of **S1**, which is identified as **pin 2** of diode **D1**).
3. Click **OK**. The net extension process will automatically add a **Series Element** between the two nets.



Extending Power Network

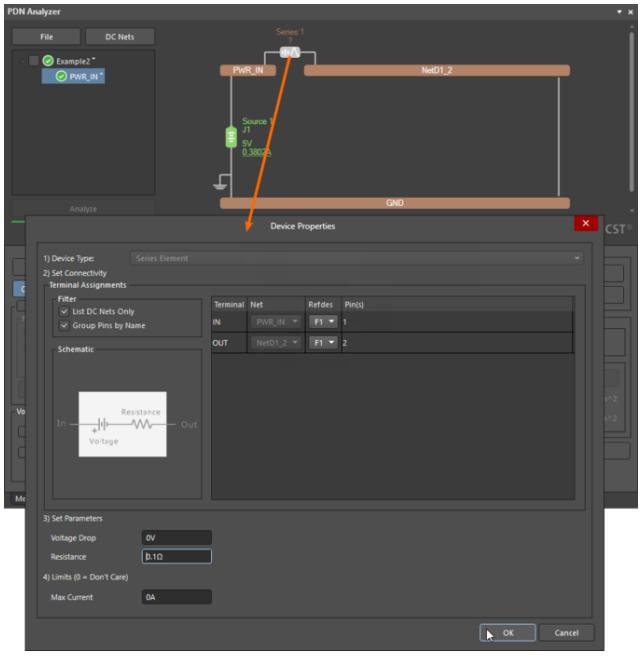
4. Double-click on the **Series Element 1** to specify **connectivity** and **parameters** in the **Device Properties** dialog.

The Series Element model is composed of a voltage source in series with a resistor, which allows the basic modeling of components such as **Resistors**, **Inductors**, **Diodes**, and **Switches** etc.

5. Set **In** and **Out** terminal's **Refdes** as **F1**.

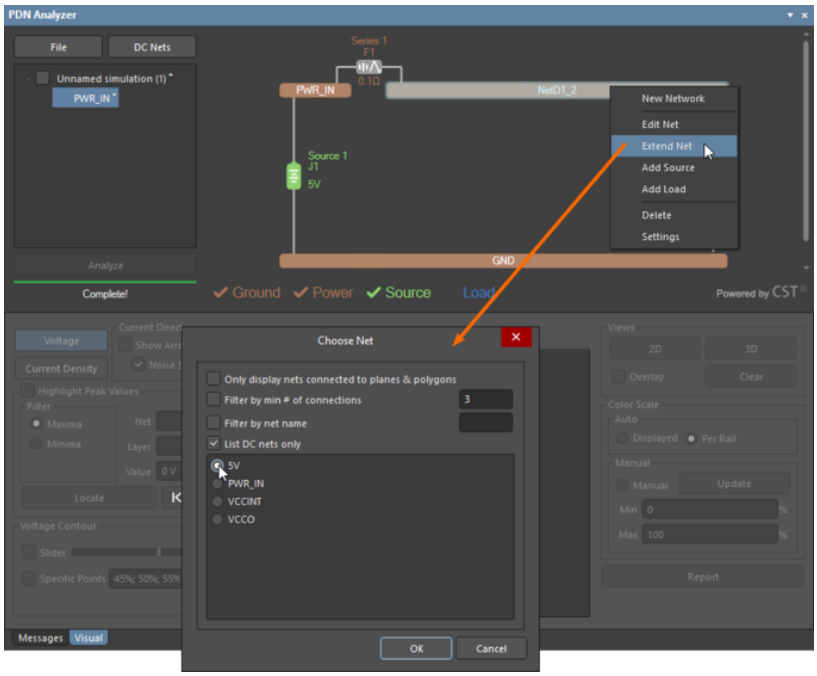
6. Set nominal internal **Resistance** to **0.1Ω** and click **OK**.

Note: If the **Series Element** was a semiconductor device, such as diode, the **Voltage Drop** parameter would be specified along with device's internal **Resistance** value.



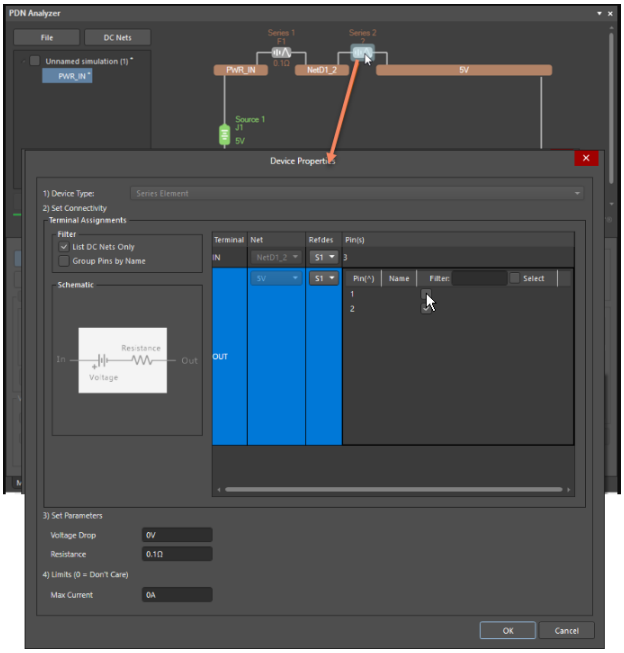
Defining Series Element Properties

7. Right-click on **NetD1_2** and select **Extend Net** from the context menu.
8. Select **5V** power net.



Extending NetD1_2 Network

9. Double-click on the **Series Element 2**.
10. Set **In** and **Out** terminal's **Refdes** as **S1**.
11. Deselect **Group Pins by Name**.
12. Disable **Pin 1**.
13. Set nominal internal **Resistance** to **0.1Ω** and click **OK**.

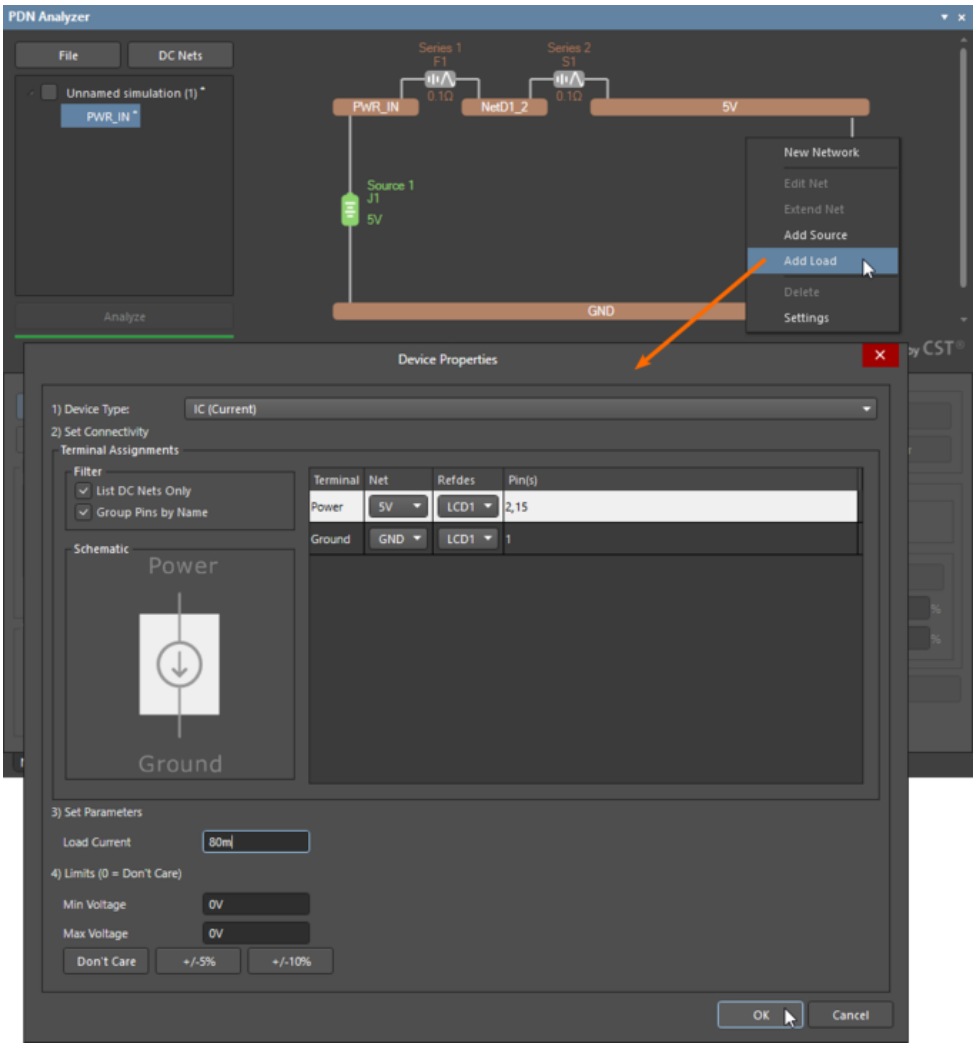


Adding Series Element 2

The added **Series Element** in this case is **S1**, which connects the **D1_2** net to the **5V** output network via **pin 2** and **pin 3**. Since the spare input switch of **S1** (**pin 1**) is tied to its output connection (**pin 2**), and does not carry load current, **pin 1** can be removed from the network analysis.

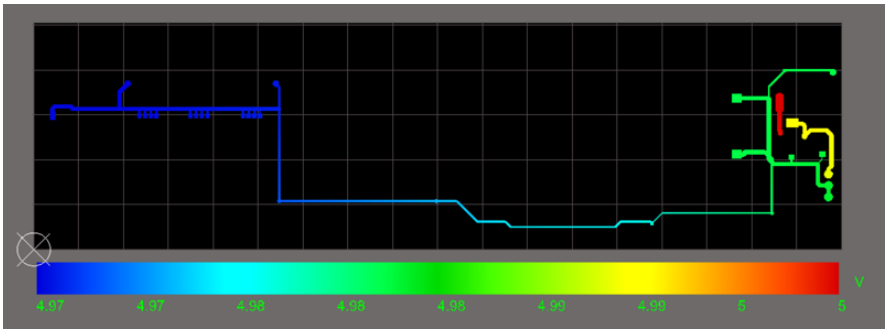
14. Add a **LCD1** as a load to the **5V** power net.

15. Set **Load Current** to **80mA** and click **OK**.



Adding LCD1 Load to 5V Power Net

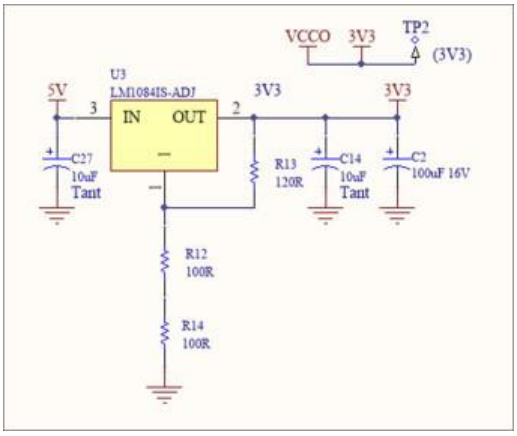
16. Initiate analysis.



Simultaneous Multi-Network Analysis

Including Voltage Regulator Models

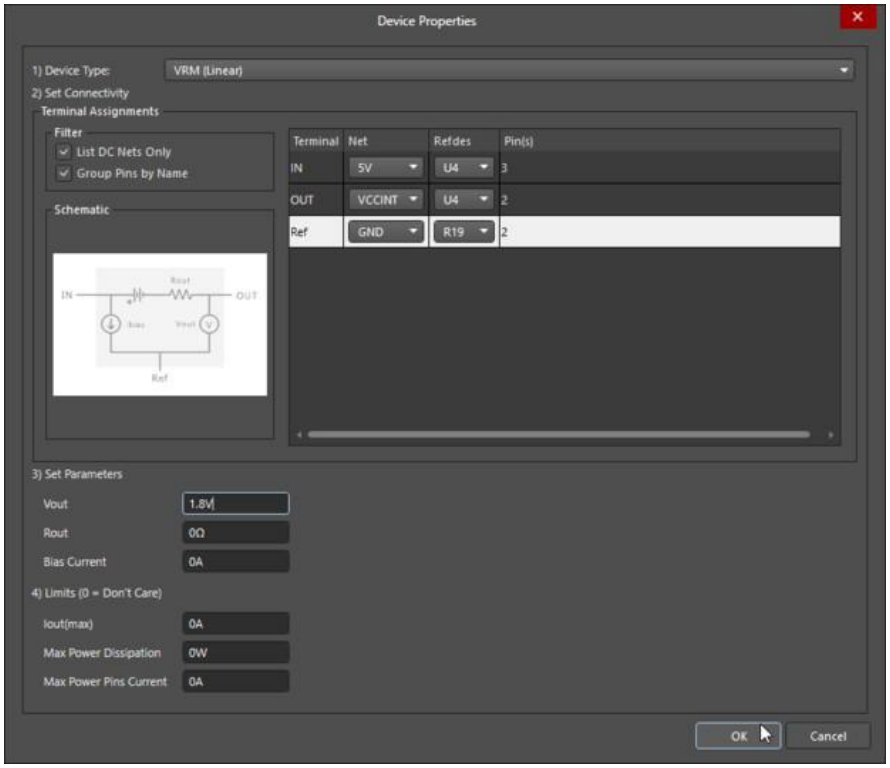
PDN Analyzer offers active **Voltage Regulator Models** (**VRMs**) that can be inserted between voltage input and output networks. When added to PDNA power networks, they manifest themselves as both a load on the voltage input network, and a source on the voltage output network. The **VRM** model options include **Linear**, **Switchmode** and **remote-sensing Switchmode voltage regulators**. Voltage regulator models (**VRMs**) are extremely powerful in PDN Analyzer because they can be defined across multiple components modeling the function of an entire regulator circuit. This allows complex and diverse designs to be easily simulated in PDN Analyzer.



Project Linear Voltage Regulator

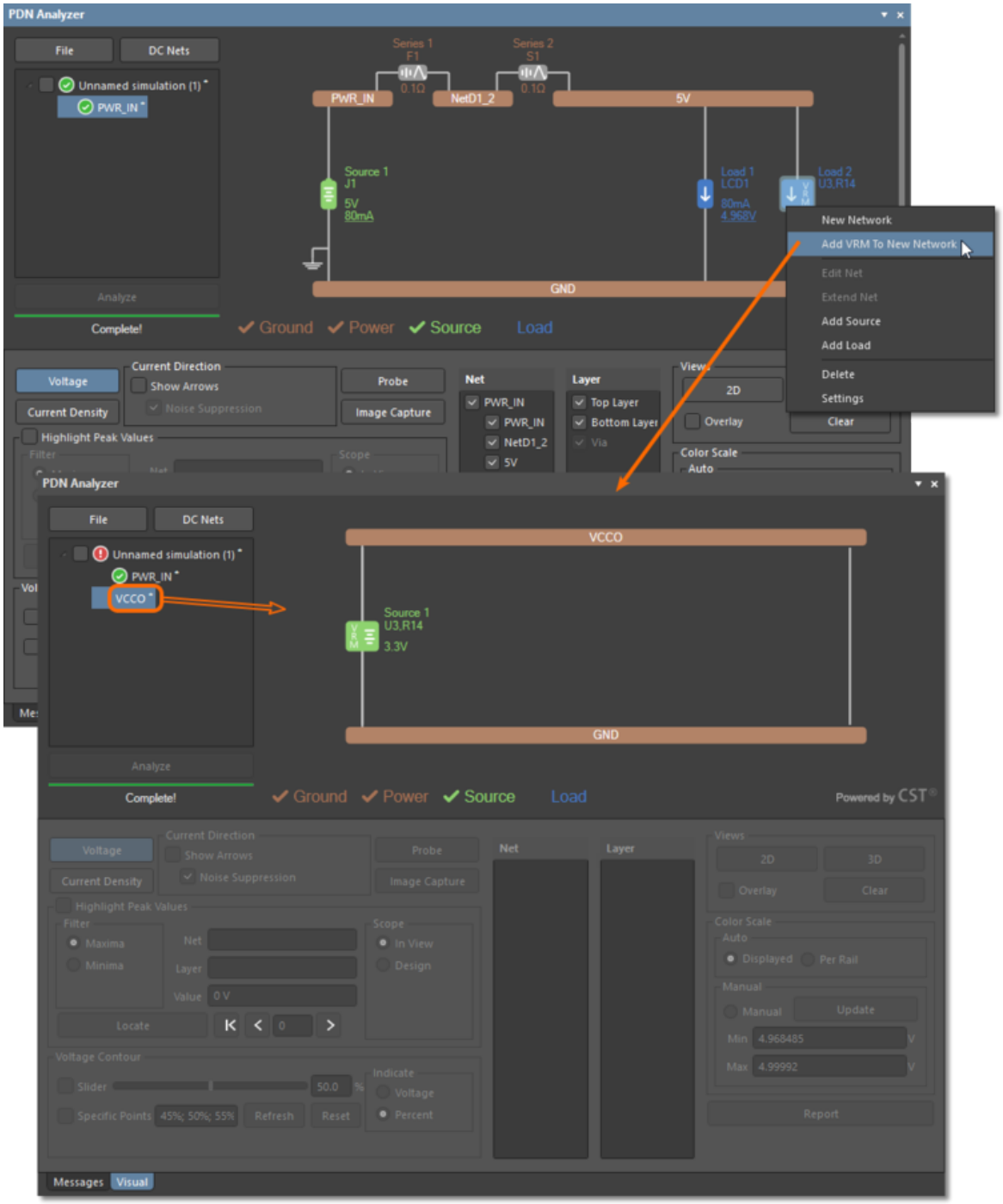
The **SpiritLevel-SL1** reference project uses **linear voltage regulators** to produce the **3.3V** (**VCCO**) and **1.8V** (**VCCINT**) power supply rails. When the **VCCO regulator** (**U3**) is added to the PDNA simulation network, it is presented as a load on the 5V input network and as a source for the **3.3V** network.

1. Add a load to the **5V** power network.
2. Select the **VRM (Linear)** option as the **Device Type** in the **Device Properties** dialog.
3. Set **In** terminal **Refdes** as **U3** and **Net** as **5V**.
4. Set **Out** terminal **Refdes** as **U3** and **Net** as **VCCO**.
5. Set **Ref** terminal **Refdes** as **R14** and **Net** as **GND**.
6. To finalize the **VRM**, set **Vout** to **3.3V** and click **OK**.



Linear VRM for VCCO Power Network

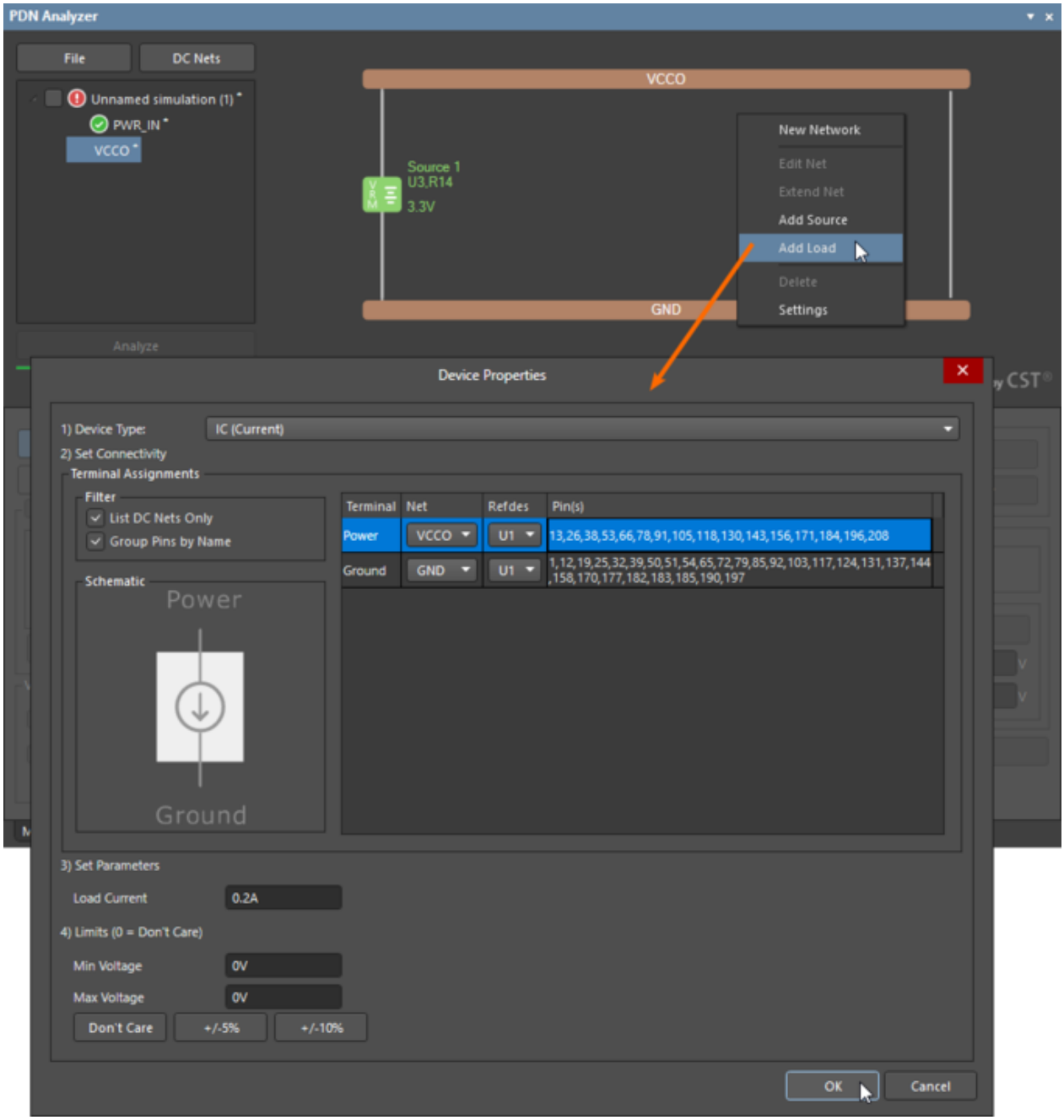
7. Right-click on the **VRM** load model that was just created **(Load 2: U3)** and select the **Add VRM To New Network** option. This will automatically create the **VCCO** network with the **VRM (Source 1: U3)** output side model as a voltage source **(3.3V)**.



Create VCCINT from VRM

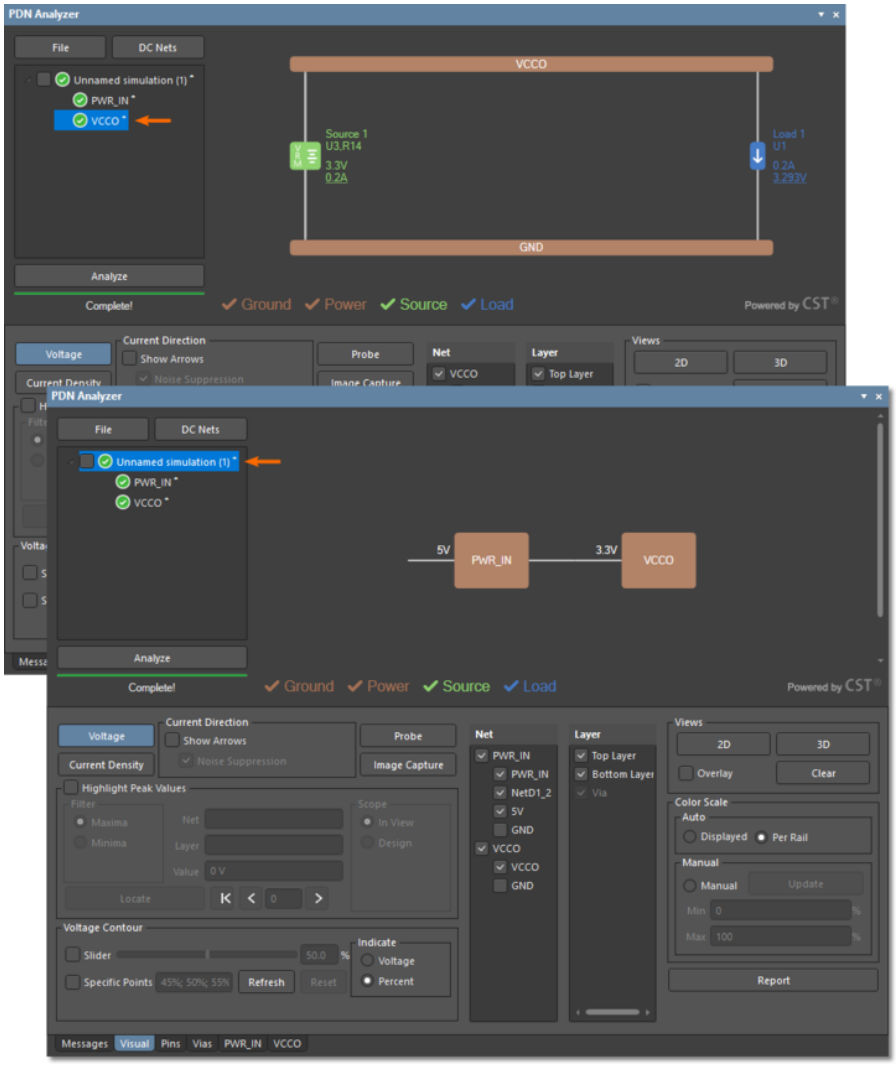
Note: The **VRM** is shared model that can be modified from any source. In this example, changes are applied bi-directionally to the Load input model reflect and the Source output model.

1. Add load **U1** to the new **VCCO** network.
2. Set **Load Current** to **0.2A** and click **OK**.



Adding a Load to VCCO VRM

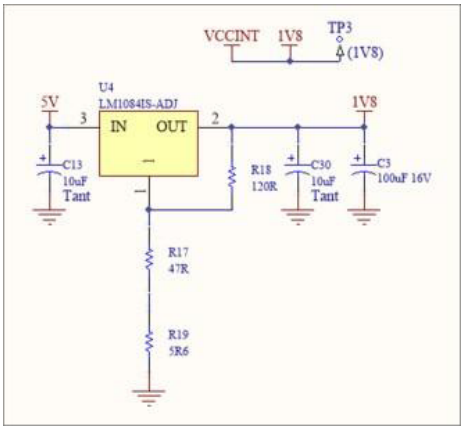
The completed power network arrangement now includes two networks **(PWR_IN** and **VCCO)** connected together by the **3.3V Linear** type **VRM**. When the top level of the network hierarchy is selected in the current PDNA file structure, the network graphic provides a block style overview of the power net interconnections. In this example the **VRM** was added as a load to the **5V (input voltage)** network, and then used to automatically create the **3.3V (VCCO)** voltage output network with the **VRM** as a **Source**. The reverse of that process is also possible. Lastly, the **VRM** is added to the **output voltage** network as a **Source**, and that model is added to an **"input" voltage** network as a **Load (Add VRM To New Network** or **Add VRM To Existing Network)**.



Network Block Overview

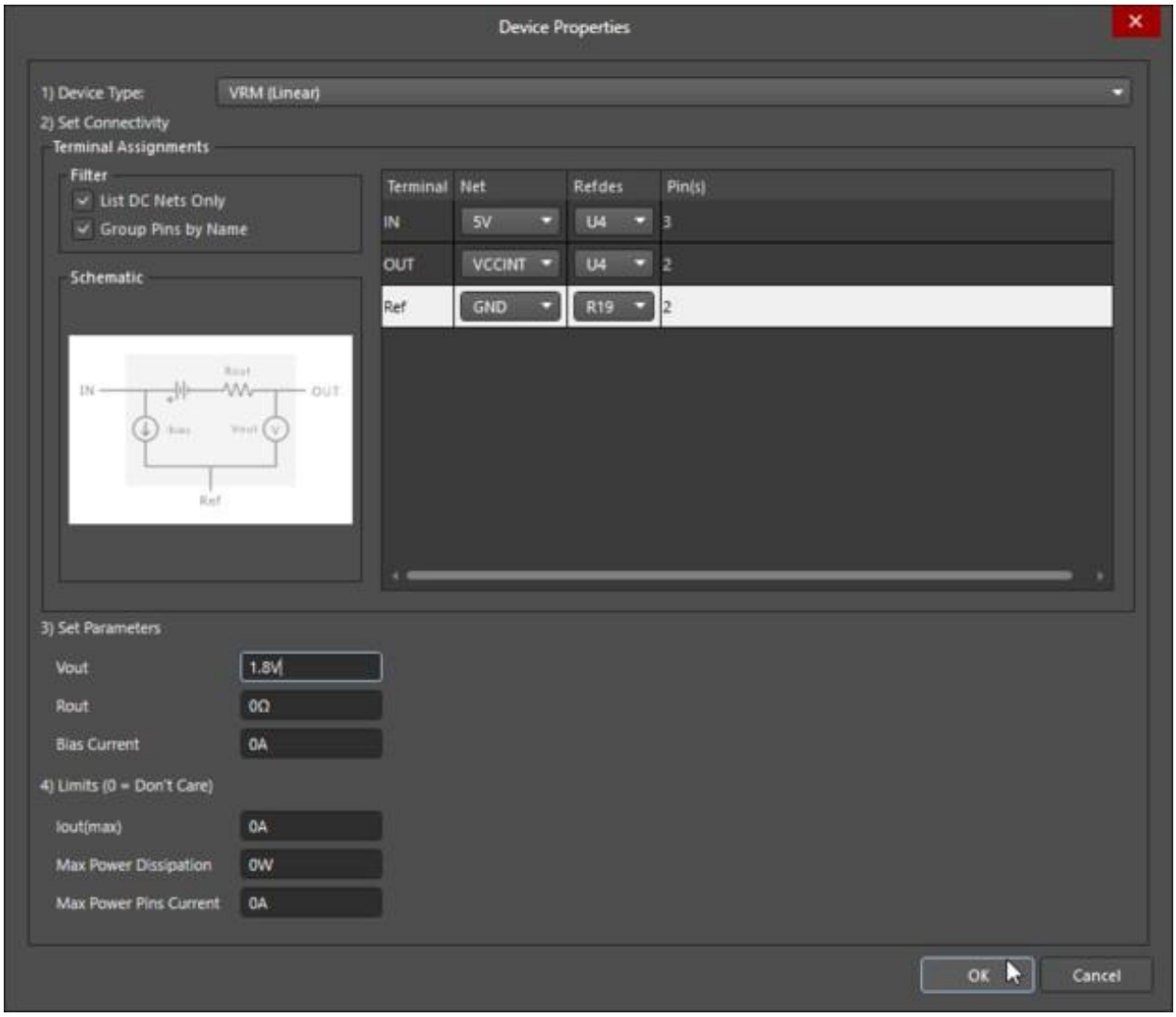
Simultaneous Multi-Network Analysis

The **GND** network path will now include return current contributions from both the **PWR_IN** and **VCCO** networks. PDN analysis will yield results for the composite network, including the **VRM**. Graphically, the PCB Editor will display all networks when the top level of the network hierarchy is selected in the PDNA interface. Adding another **VRM (U4)** will complete the example project's power distribution network and incorporate the **1.8V** power output network **(VCCINT)**.



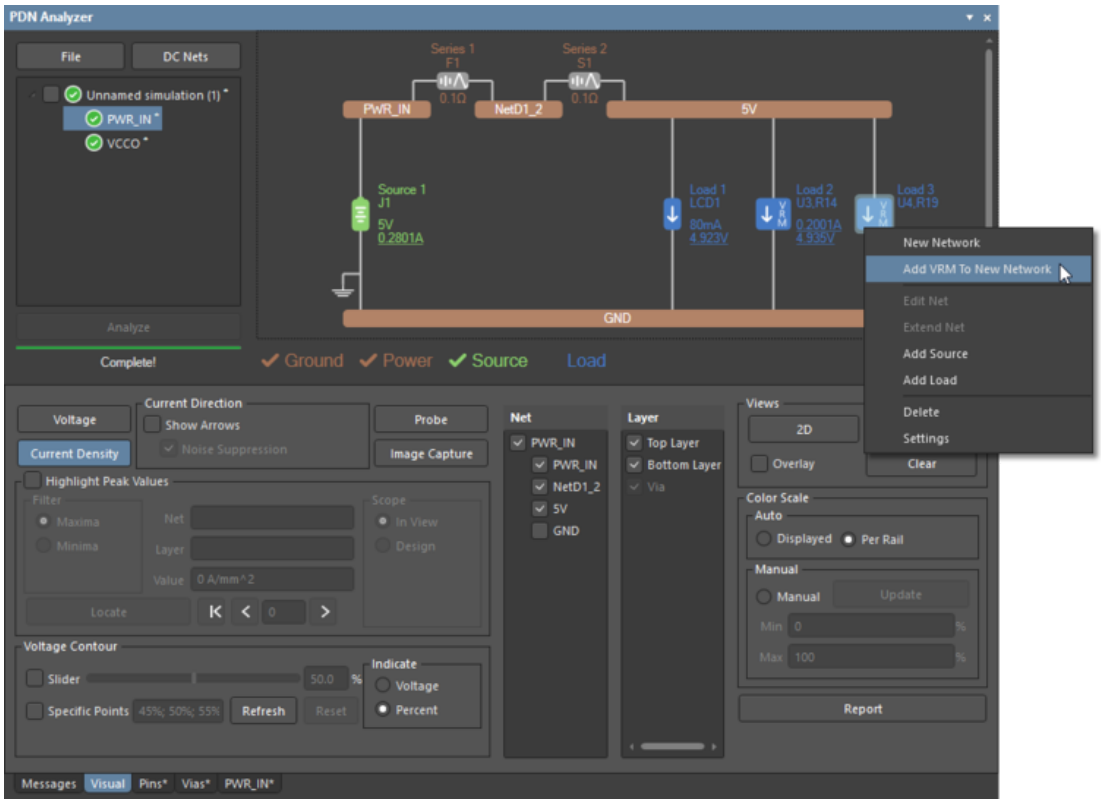
Second Power Network Linear VRM

1. Click on Network Simulation Setup, **PWR_IN**.
2. Add a **Linear VRM** to the **5V** network with the following parameters.
    a. Set **In** terminal **Refdes** as **U4** and **Net** as **5V**.
    b. Set **Out** terminal **Refdes** as **U4** and **Net** as **VCCINT**.
    c. Set **Ref** terminal **Refdes** as **R19** and **Net** as **GND**.
    d. Set **Vout** to **1.8V**.
3. To finalize the **VRM**, click **OK**.



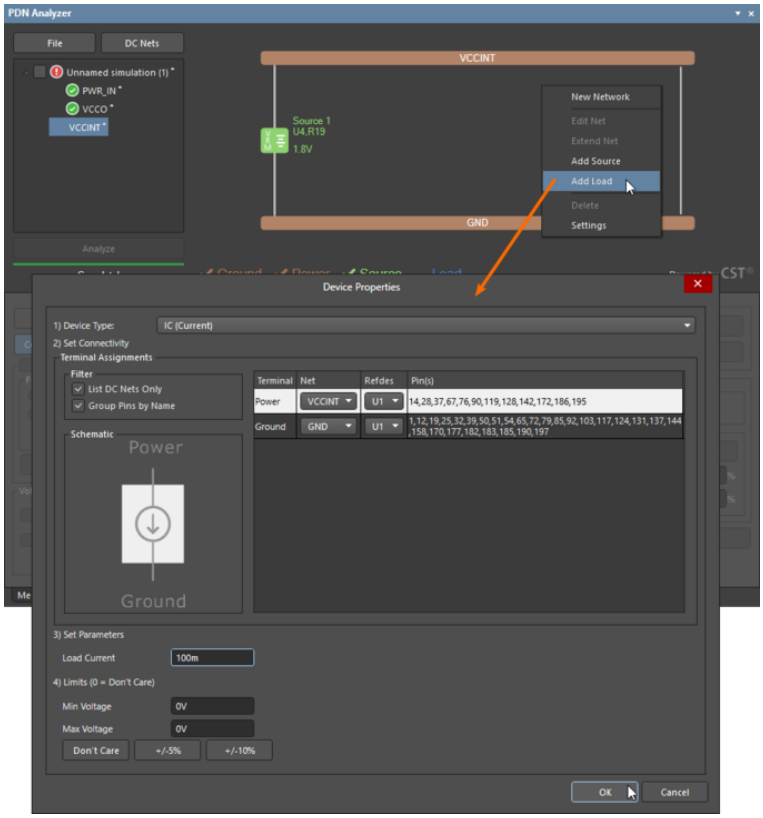
Linear VRM for VCCINT Power Network

4. Add the **VRM Load 3** to a new network to create the **1.8V (VCCINT)** power network.



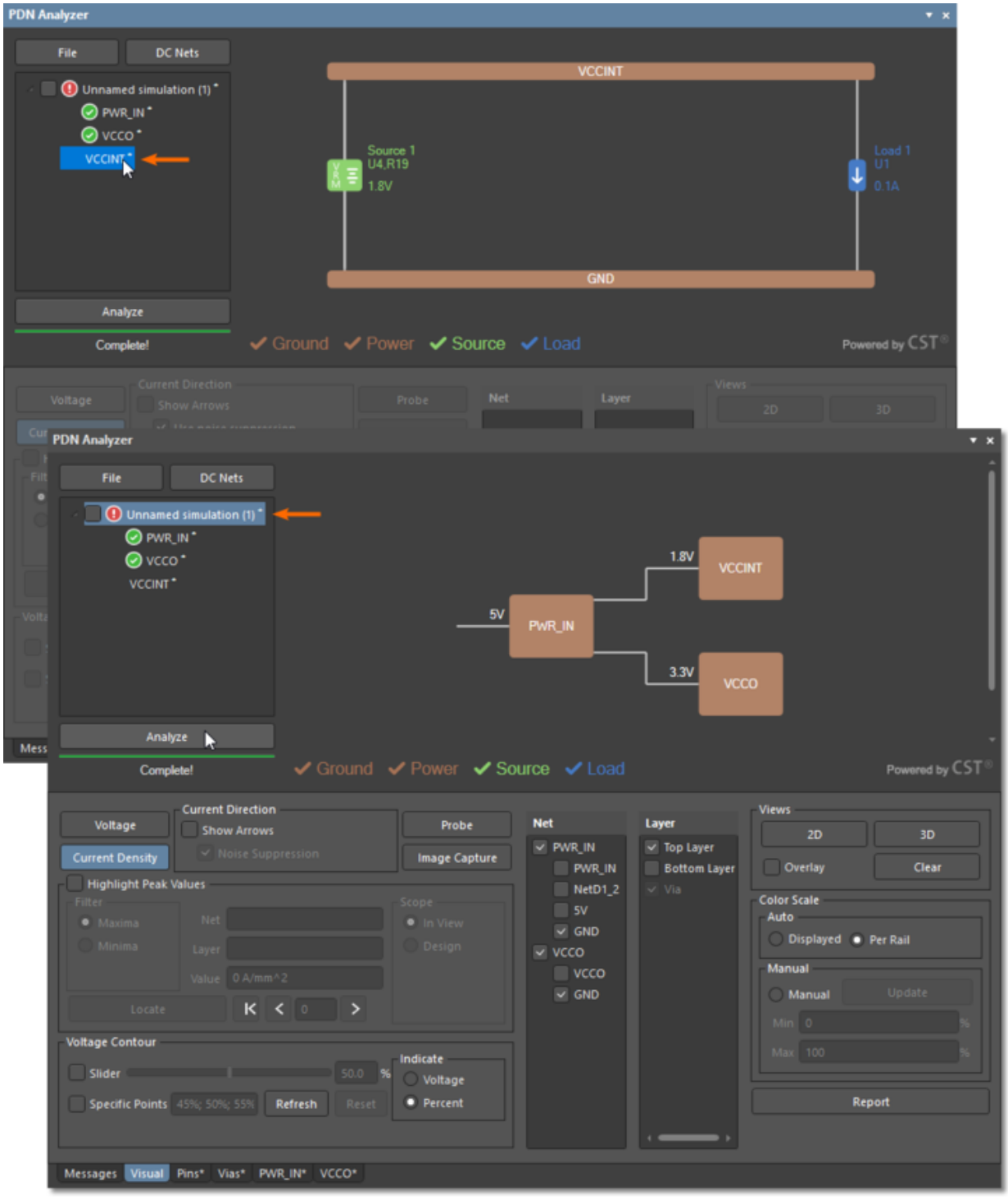
Create VCCINT from VRM

5. **Add Load U1** to the **VCCINT** network.
6. Set **Load Current** to **100mA** and click **OK**.



Adding a Load to VCCINT VRM

7. Right-click on network simulation setup, **Unnamed simulation(1)**, and select **Save As**.

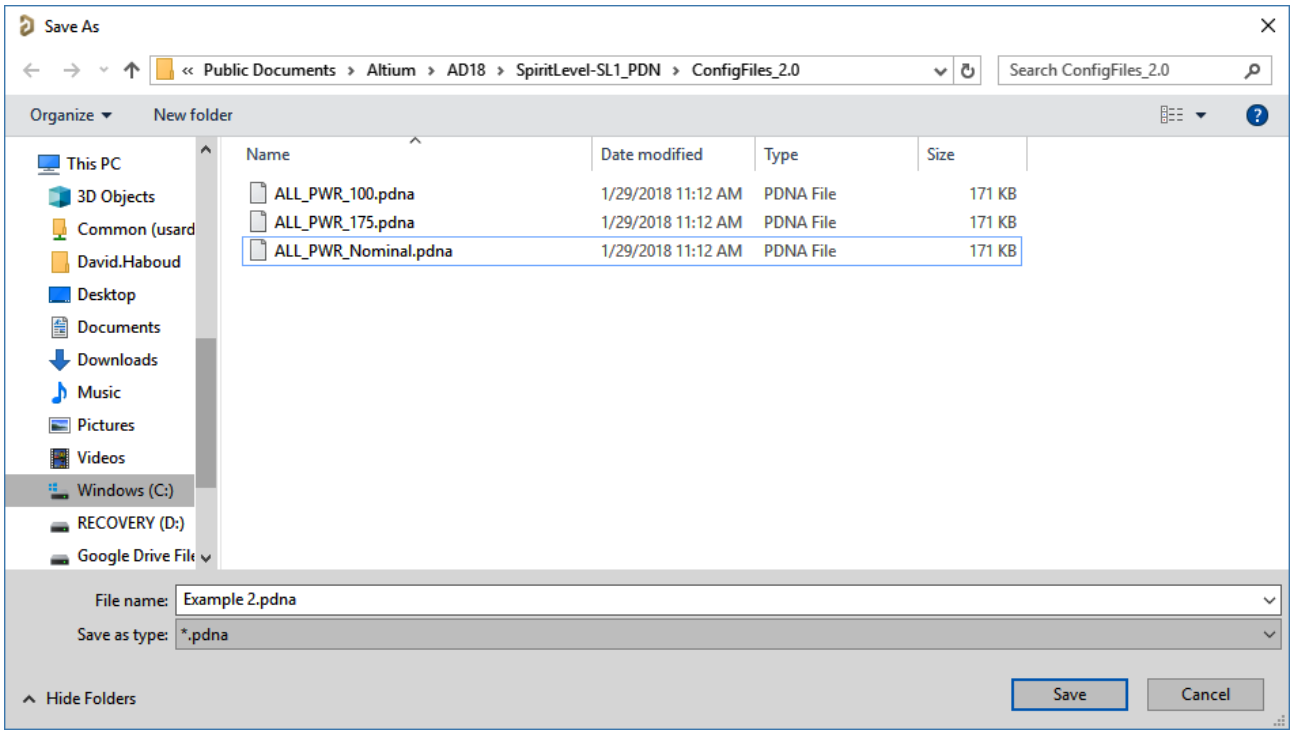


Simultaneous Multi-Network Hierarchy

8. Select folder **ConfigFiles_2.0** in the project directory.

9. Save file name as **Example 2**.

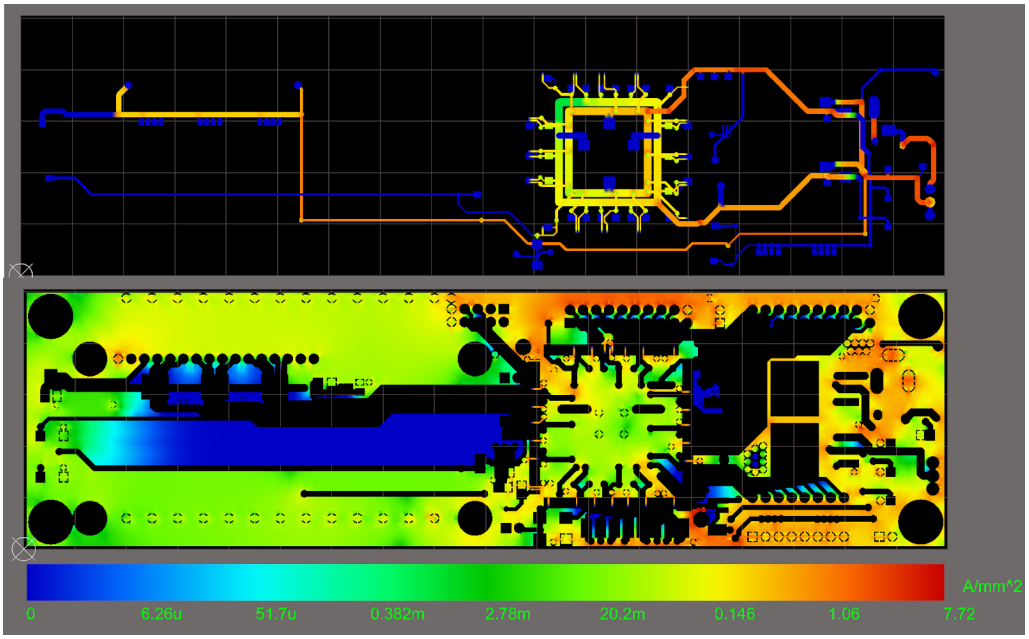
Note: A PDN configuration is a file (*.pdna) which captures and saves all user settings and values specified within an existing analysis setup. Configuration files enable you to save and manage any number of analysis setups for subsequent use.



Saving Configuration File

10. Initiate analysis.

The PDNA interface network hierarchy shows all three interconnected networks. PDN analysis will yield results for the composite network, including the **VRMs**. The **GND** network now includes the return current for all three networks, which use the common **GND** layer shapes.



Visual Simultaneous Multi-Network PDN Analysis

EXAMPLE 3 - LIMIT ANALYSIS ON SIMULTANEOUS MULTI-NETWORK SIMULATIONS

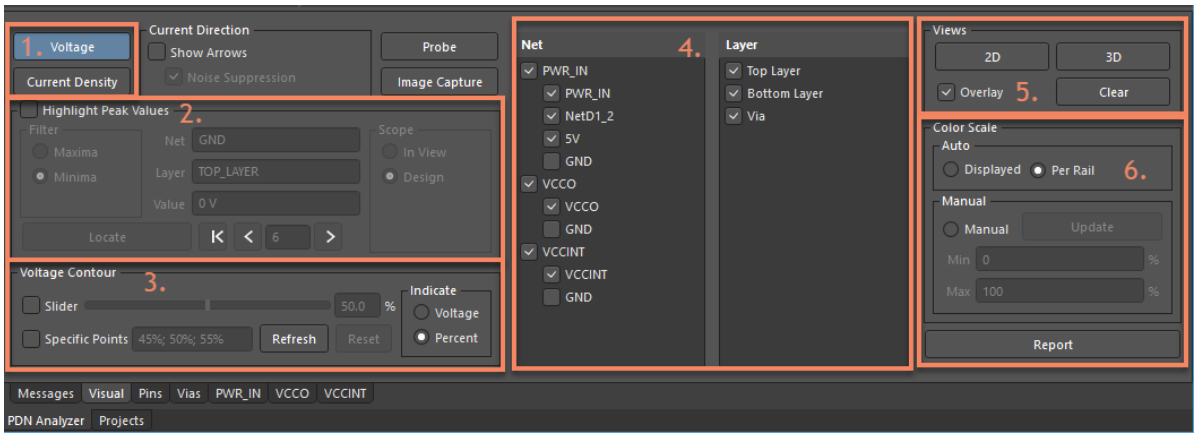
In this example we will load a completed configuration file and review the special analysis capabilities of PDN Analyzer. When analysis has completed, the lower half of the PDN Analyzer panel will enable several viewing and reporting functions. In the top half of the panel, red or green status icons indicate limit check status in the power delivery network.

1. Select the **File >> Open** to navigate to the **ConfigFiles_2.0** folder and choose the existing **ALL_PWR_Nominal.pdna** configuration file.
2. Select the **ALL_PWR_Nominal** network setup to load the existing PDN configuration.
3. Initiate analysis with the **Analyze** button.

Of the three power rails in this design, the **1.8V (VCCINT)** rail has a limit check failure as indicated by the dashed red outline around the **VCCINT** symbol, as well as the red status icon to the left of the **VCCINT** network listed in the upper left corner. We will explore and resolve the limit check failure in later steps of this guide.

The **Results Pane** is organized in the following sections:

1. **Display Filters**: Used to control the mutually exclusive display of either voltage level or current density results in the actual PCB layout. Current direction arrows can be enabled here to indicate the flow of current within the layout.
2. **Highlight Peak Values**: Provides the ability to locate, highlight, and zoom to peak values (i.e., lowest voltage, highest current density). Also provides the ability to move to the next successively (least/most) value.
3. **Voltage Contour**: Enables the marking of specific voltage or percent points within the layout.
4. **Net and Layer**: Enables the display of PDN Analyzer results of specific nets and layers
5. **Views**: Enables the display of PDN Analyzer results as 2D or 3D. Overlay option provides display of non-PDN specific objects as a visual context. A Clear button deletes the display of all PDN Analyzer results within the PCB layout.
6. **Color Scale**: Controls the color gradient representation of voltage or current density information.



Initial Results - Visual Tab

Analyzing Simulation Failures

Now let's view the voltage drop results for the failed **VCCINT** net.

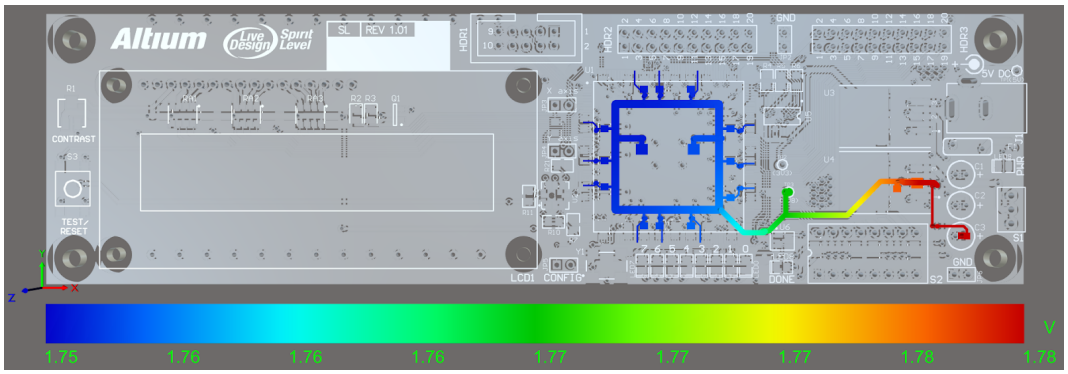
1. Double-click on the **1.8V (VCCINT)** symbol outlined with a dashed red line.

Note: Selecting a single power network will allow you to focus on the source and loads in the network, while maintaining the effects from the other network interconnections.

2. Make sure **Voltage** mode is selected.
3. Disable the **GND** net and enable all layers.
4. In the **Views** section, click the **3D** button and enable the **Overlay** option.

Note: **3D** mode enables the **Via** layer that is unavailable in **2D** mode.

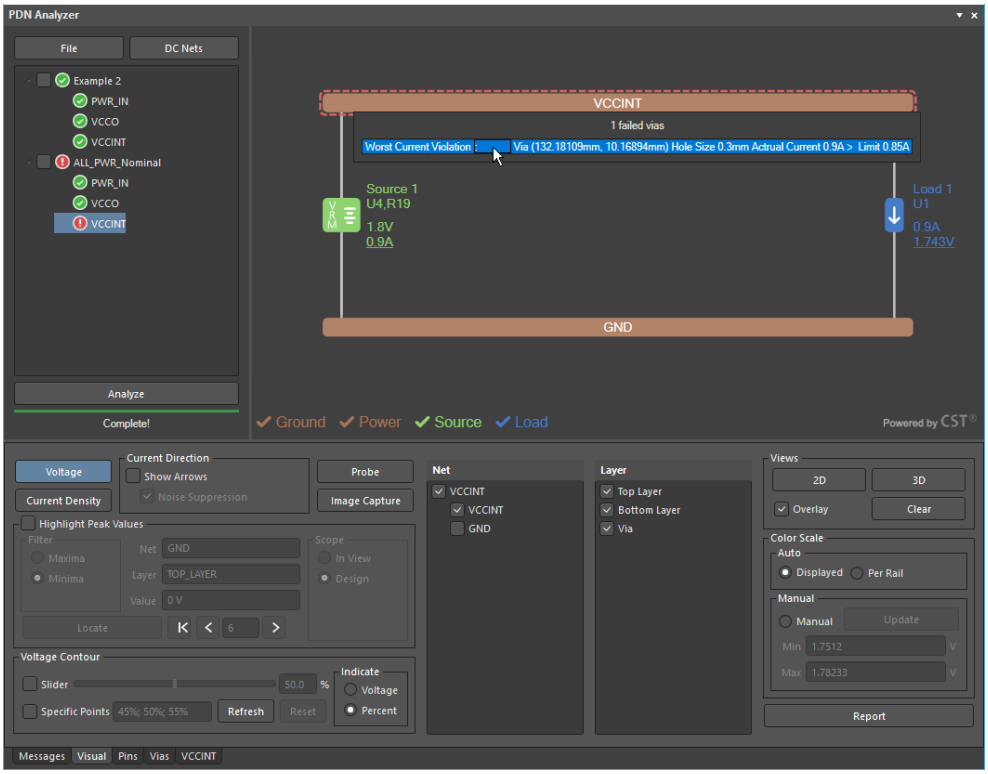
5. In the **Color Scale** section, check the **Displayed** option in order to display the legend as volts.



*VCCINT Voltage Drop Results in **3D** Mode*

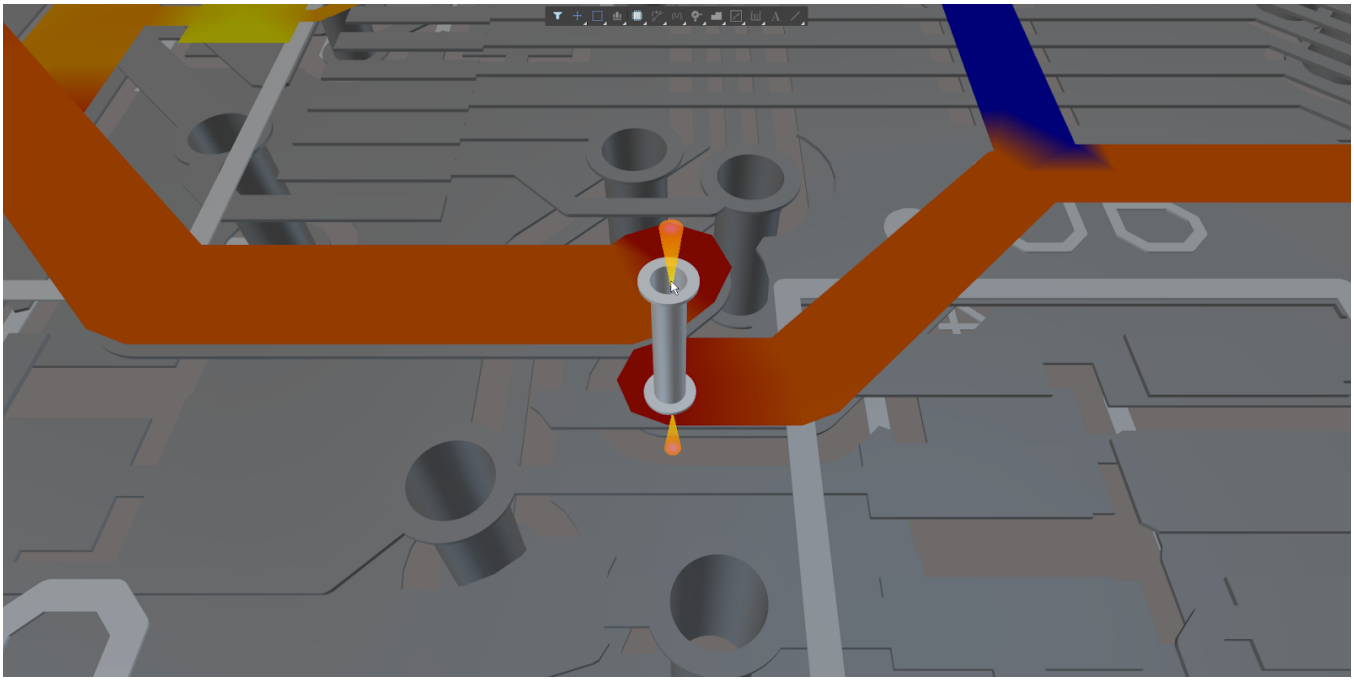
Now observe the results within the PCB Editor, you should see a display similar to the image above. The legend shows the color gradient representing the maximum voltage at 1.78 VDC and the minimum voltage at 1.75. Notice how the voltage is highest at the voltage regulator source component (**U4**) and lowest at the furthest extents of the load component (**U1**) routing.

6. Hover cursor over the failed **VCCINT** until the violation message appears.
7. Double-click on the violation message to cross-probe to the violation on the board.



Worst Current Violation

8. Switch to **Current Density** mode.



Worst Current Violation

Now let's view the current density results for the **VCCINT** net in more detail. Now observe the results within the PCB Editor, you should see a display similar to the image above. The legend shows the color gradient representing the maximum current density for **VCCINT** at **175 A/mm^2** and a minimum current density of **0 A/mm^2**. Notice how the current density is highest at certain points in the power trace and lowest (0) at point where there is no DC load (such as at the pins of decoupling capacitors).

Other Violations

Along with the detection of defined **Current Violations**, PDN Analyzer will detect a wide range of other network performance violations, such as any **Limit** parameters that have been specified when adding a **Load**, **Source**, or **Series Element**. All changes made to **Limits** take effect immediately to existing results.

These parameters include:

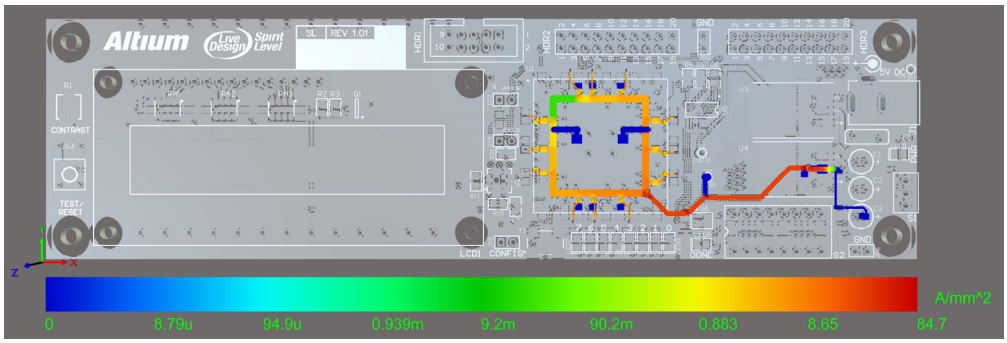
- The acceptable **voltage range** at a **Load**.
- The maximum **output current** from a **Source**.
- The permitted **power dissipation** in a **Linear Regulator Source** and its maximum output current.
- The maximum **output current** from a **Switchmode Regulator Source**.
- The maximum **current** through a **Series Element**.
- Where a **Limit** parameter has been specified (has a non-zero value), a violation of the parameter will cause the offending network element to be highlighted in the PDNA interface network graphic. Hover the cursor over the element to see its parameters and analysis results.

More detailed information on the performance of a power network is available under its network tab, which presents a tabular view of the analysis results data and includes computed network power consumption values.

Modifying and Reanalyzing The Design

One of the main benefits of PDN Analyzer is that the setup and analysis can performed without having to leave the PCB editor. This makes it easy to perform successive modify/analyze iterations during the layout process. As observed earlier, the via at location (X=132.18109, Y=10.16894) was both called out in a **Worst Current Violation** and shows as the point of highest current density in the design. The 0.3mm hole size and 0.5mm diameter result in a bottleneck in the path between the source of **VCCINT** and the load component **U1**. Consequently, the current density is very high which could result in excessive heat, or worst case fuse open.

1. Click the **2D** button then the **Clear** button within the **Views** section.
2. Double-click on the via to edit its properties (location X=132.18109, Y=10.16894).
3. Change the **Hole Size** of the via from **0.3mm** to **0.6mm**.
4. Similarly change the **Diameter** of the via from **0.5mm** to **0.9mm**.
5. Initiate analysis again and view the current density mode for net **VCCINT**.



Analysis After Via Violation Modification

Notice this time the **Worst Current Violation** no longer occurs. Additionally, the maximum current density in **VCCINT** has now dropped from **175 A/mm^2** down to **84.7 A/mm^2**. Such iterations are common in the process of optimizing for the lowest current density and voltage drop between the sources and all loads. A design that is thoroughly optimized for the lowest current density and voltage drop will generate less heat and have less chance of elevated temperature influenced issues in the field. PDN Analyzer enables such optimization directly within the PCB editor early and throughout the layout process.

Identifying Power Integrity Points of Interest

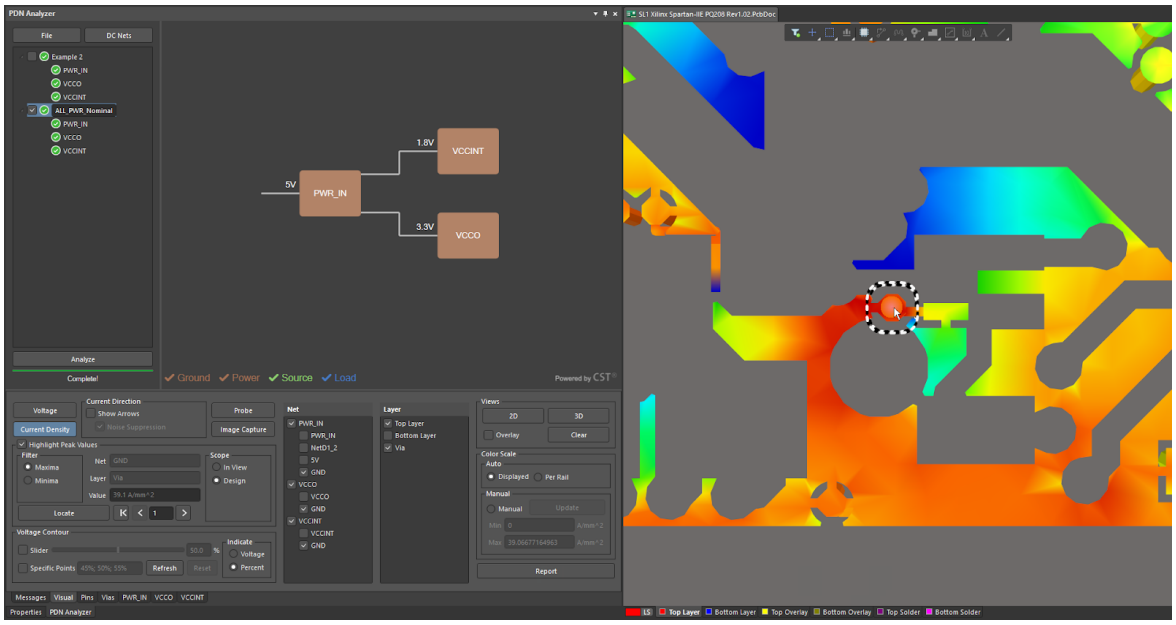
PDN Analyzer offers a comprehensive range of graphical and data information that can be used to assess and troubleshoot the power integrity of an analyzed PCB design. Taking the example shown above, the analysis of the **Top Layer GND** network path indicates the possibility of a current density hotspot, as indicated by the maximum scale reading of **39.1 A/mm²** and the current density gradient approaching the via. The location of the problem area is not immediately obvious, but can be exposed using the **Highlight Peak Values** and **Current Directional Arrows** features.

Highlight Peak Values

1. Select the **Current Density** view.
2. Switch to **3D** View.
3. Toggle display settings to all show only **GND** net.
4. Enable the **Top Layer** and **Via Layer**.

5. Enable **Highlight Peak Values** in the **Visual** tab.
6. Set the **Scope** option to **Design** to pan and zoom to each location as you step through the entire layout.
7. Set **Filter** option set to **Maxima**. The peak *current density* area will be highlighted and marked on the analysis graphic in the PCB Editor.
8. Click the Locate button to repeat the graphic highlighting. This shows you the area with the highest current density.

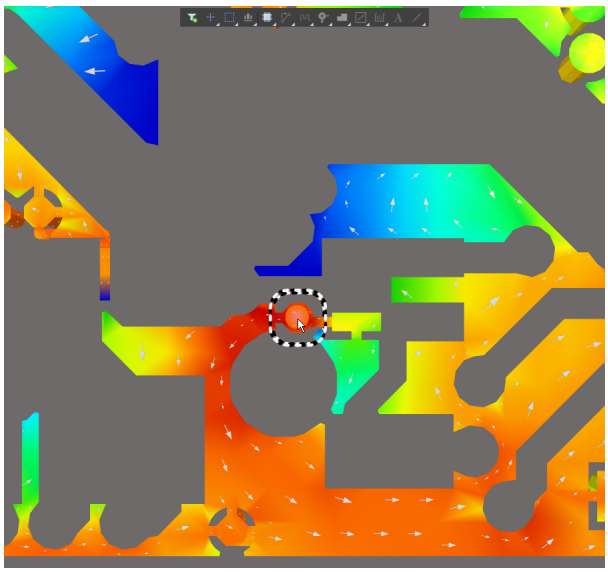
Note: You can use the associated buttons to step through the peak readings/locations in order.



Highlighting Errors

Current Directional Arrows

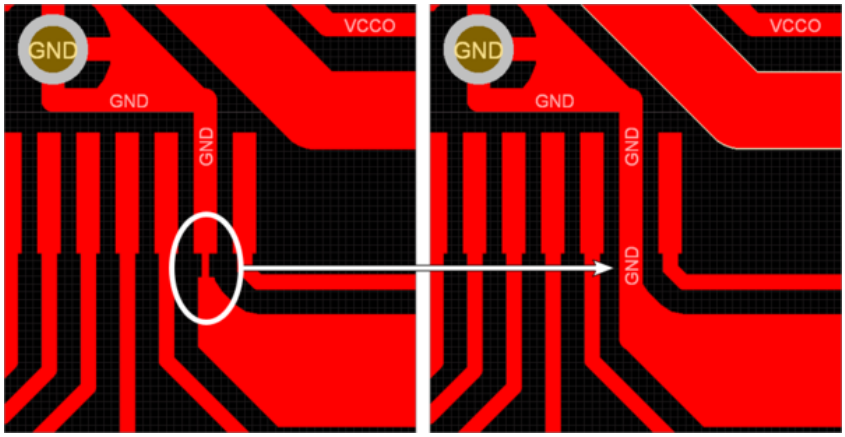
Further information about an area of concern can be deduced by enabling the **Show Arrows** feature, which overlays multiple arrow graphics that indicate *current direction* (arrow's angle) and the *relative magnitude* (arrow's size) at that location. For this example, it confirms that the current flow is not optimal to distribute current density across the **GND** copper.



High Current Density Area

One way to resolve this issue is to connect the **U1 GND pin 103** to the larger ground plane to improve current flow. The PCB edit can be completed while **PDN Analyzer** is active, which allows iterative layout improvement to be completed and then re-analyzed.

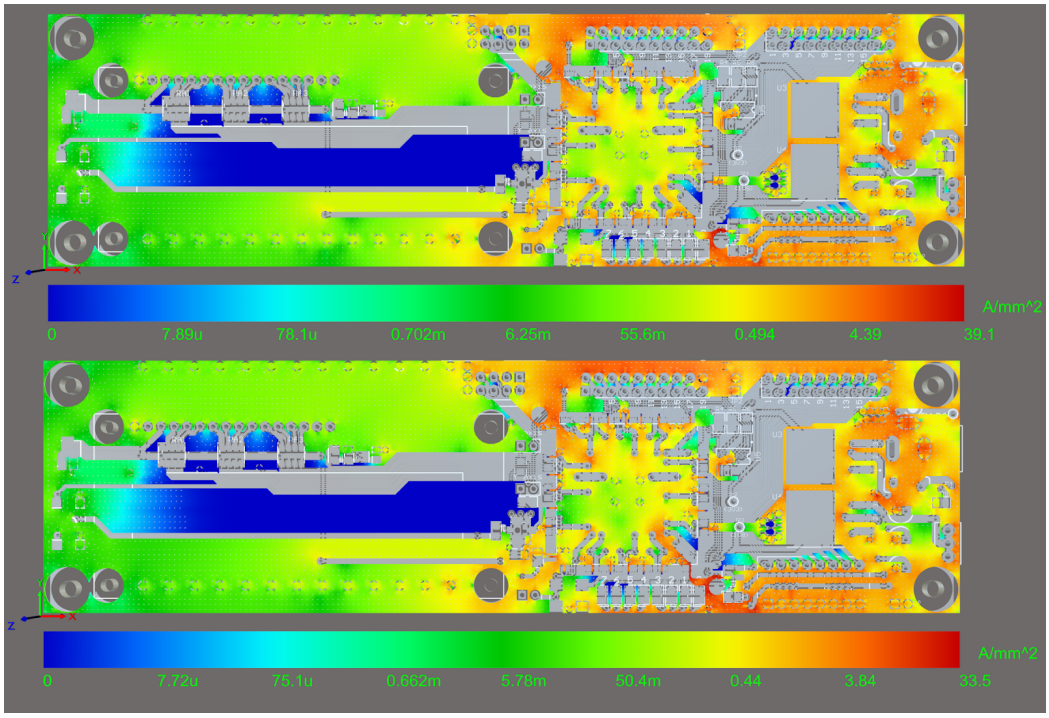
1. Click the **Clear** button in the **Views** area to disable the **PDNA** results in the PCB Editor.
2. Connect **U1 GND pin 103** to the **GND** copper with default settings (0.3mm).



Connecting GND Pin

3. Click Analyze to rerun analysis and check the power integrity results.

The below two images illustrate the change in current density through the **GND** network (on the **Top Layer**) due to the connection of the **GND** pin at that critical point – the upper image shows the initial **Current Density** result, while the lower image shows the **Current Density** graphic after the PCB modification. For a more literal graphic comparison, manually set the **Current Density** scale to the previous value – select the **Manual** scale option, enter **33.5** in the **Max** field and click the Update button to refresh the display.



Current Density Analysis Comparison

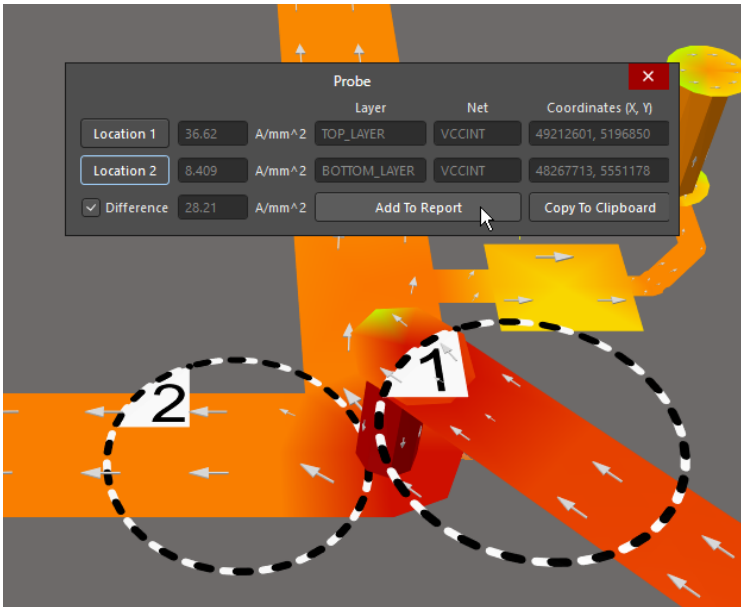
Data Probe and Image Capture

Along with the visual interpretation of the PDNA analysis graphics and **Scale** in the PCB Editor, the **Probe** tool helps interpret the analysis results at specific points in the design layout. The **Probe** tool allows the **Voltage** or **Current Density** data at nominated points in the design layout to be recorded and compared. The versatility of the tool provides a method to accurately judge the analysed data results on any network or layer. We will perform a difference probe reading for the current density on the **VCCINT** network.

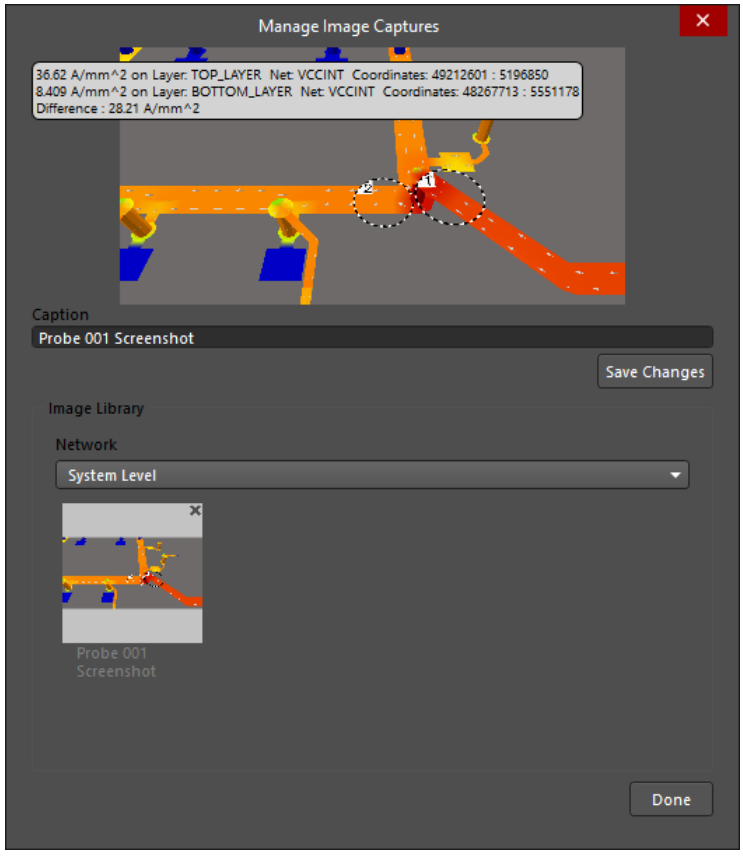
1. Enable only the **VCCINT** power net.
2. Enable all layers.
3. Select **Current Density** mode.
4. Enable **Current Direction** arrows.
5. Select the **Probe** button to open the **Probe** dialog.
6. Enable the first probe location, **Location 1**.
7. Use the cursor crosshair to nominate the top trace entering the via at the corner of **U1**.
8. Check the **Difference** option and nominate the second location, **Location 2**.
9. Use the cursor crosshair to nominate the bottom trace entering the via at the corner of **U1**.
10. Click **Add to Report**.
11. Edit the **Caption** to describe the image: "Probe 001 Screenshot"

Note: It is recommended you are make the caption very descriptive to make the intent clear to your manufacturer.

12. Select **Save Changes**.
13. Click **Done**.



Probe Differences



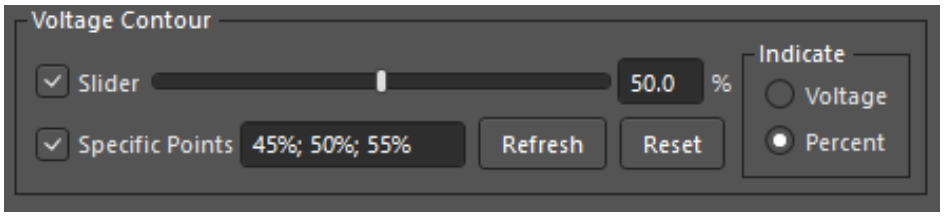
Adding Probe Image to Analysis Report

Voltage Contour

The **Voltage Contour** feature allow you to find the best location to place remote sensing lines. The feature enables an overlay of dashed voltage contour lines through the displayed layers in the PCB Editor graphics to indicate key voltage transition points in the board layout. Multiple contour lines can be specified and displayed as either a percentage of the network voltage drop or as literal voltages. Along with the set of contour lines at specified percentage points, a further line may be included using the **Slider** option, which provides a continuous adjustment method of setting a line transition point.

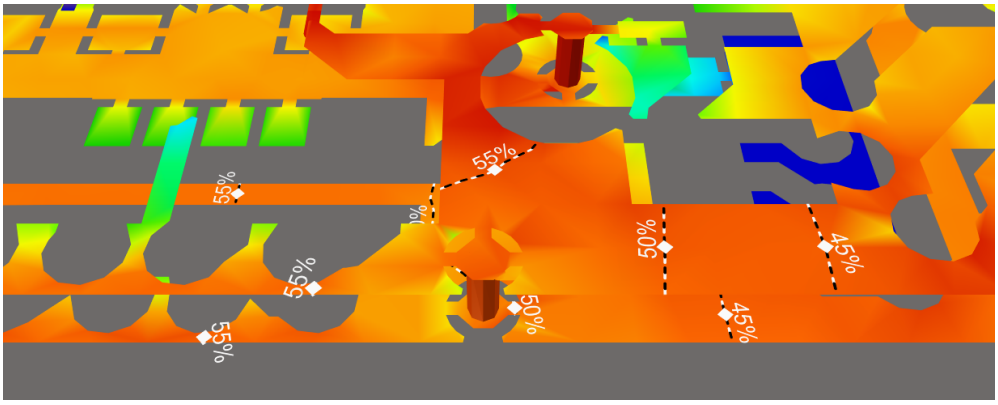
1. Enable only the **VCCINT GND** net.
2. Enable all layers.
3. Select **Voltage** mode.
4. Enable the **Slider** and **Specific Points** check boxes.

Note: The **Slider** can be moved in 1% increments by clicking to the left or right of the slider, or in 0.1% increments by using the left/right keyboard arrows. Voltage values can be directly entered and combined with percentages into the **Specific Points** field - e.g. "53% 2.2m".



Voltage Contour View

5. Navigate to the bottom of the design.

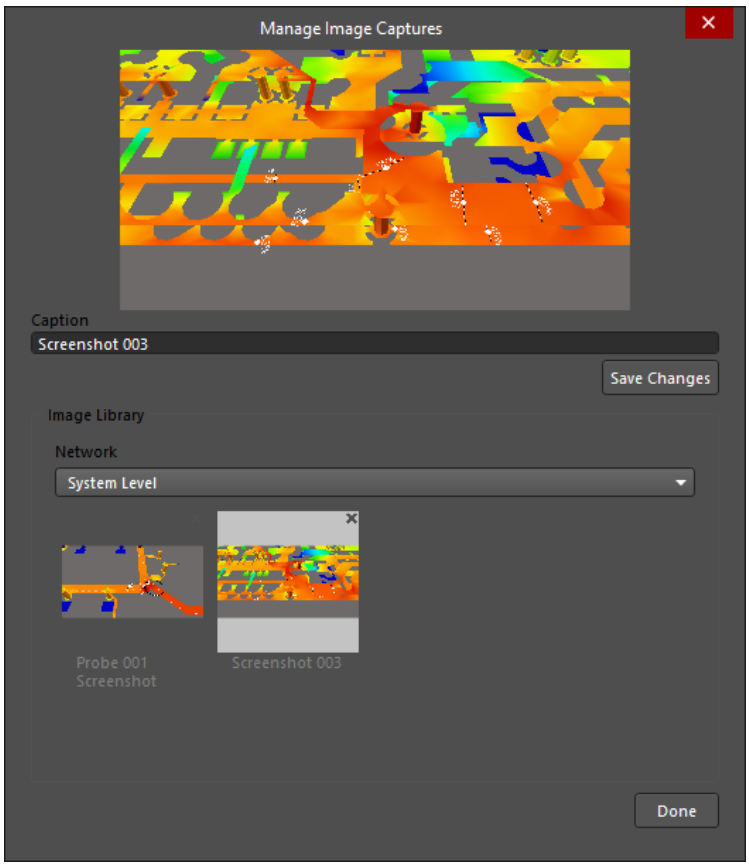


Voltage Contour Lines

Analysis Report

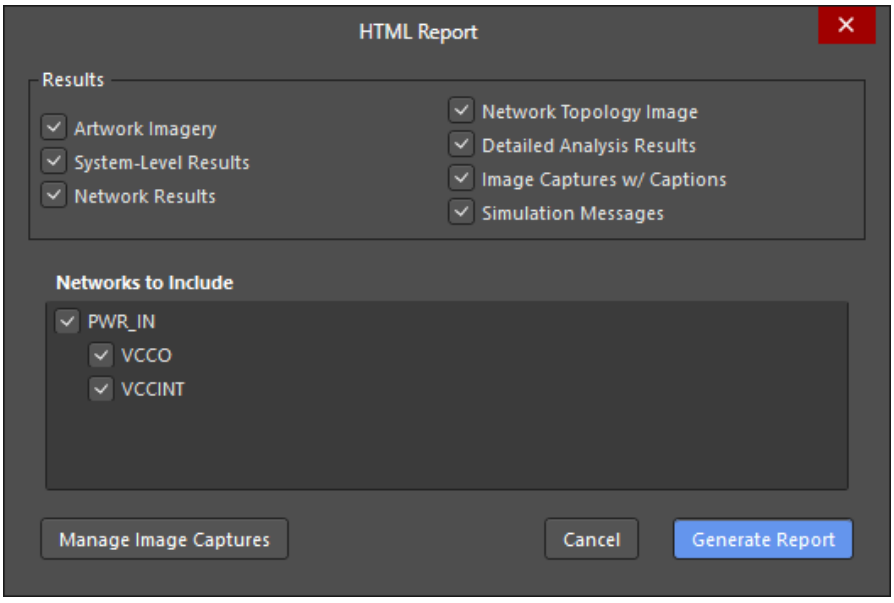
To store the results of a power integrity analysis for further examination or distribution to stakeholders, **PDN Analyzer** offers a data and documentation **Report** function. The **Report** feature generates a very comprehensive **HTML-based** document that includes graphics and data for both current analysis results and the board design itself. We will add an image capture of the voltage contour lines to the report.

1. Click **Image Capture** in the **Visual** tab.
2. Click **Done**.



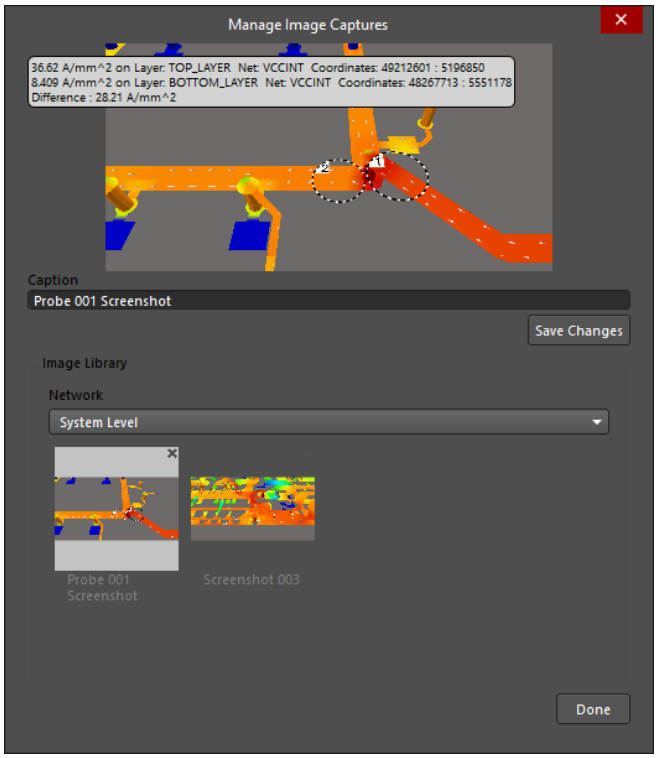
Adding Image Capture

3. Select **Report** button to configure the **Report** options in the **HTML Report** dialog.
4. Check the **Results** inclusion boxes to set the degree of detail included in the **Report**.



HTML Report Dialog

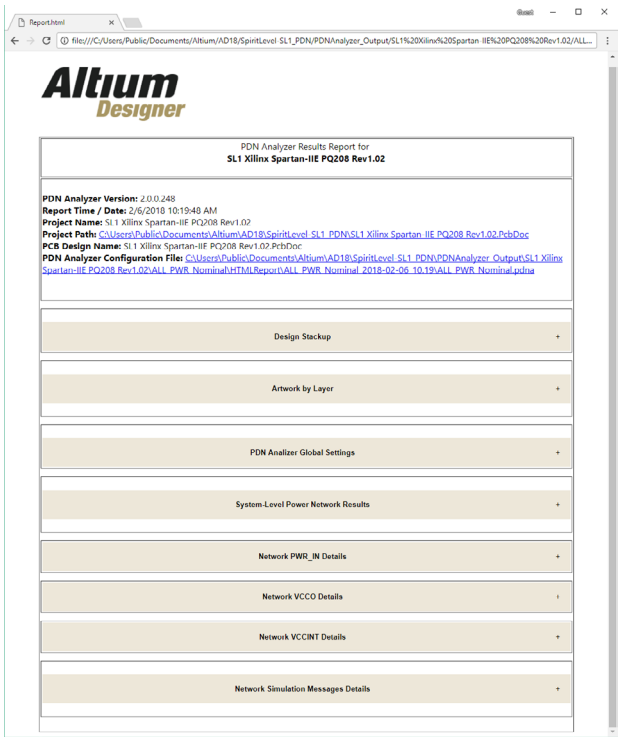
5. Click **Manage Image Captures** to review any captured images to be included in the **Report** folder and click **Done** when finished reviewing.



Managing Report Image Captures

6. Click the **Generate Report** button to generate the interactive HTML Report and open its host folder, which will include all images (including those captured) and the related analysis configuration file **(*.pdna)**.

7. Open the **HTML** report form the Windows Explorer.



HTML Report

Batch Configuration Analysis

Batch simulation allows easy corner case analysis. For example, temperature variations can be configured and saved as multiple configuration files where each configuration has a different ambient temperature value specified. In the PDN Analyzer panel, one or more configuration files can be loaded and subsequently run either individually, or as a batch of any number of multiple configurations. Results for each unique configuration are saved in a subfolder and can be viewed directly at any time. The main benefit here is that many configurations can be run, and the results of each configuration can be viewed at any time—even after exiting and restarting Altium Designer.

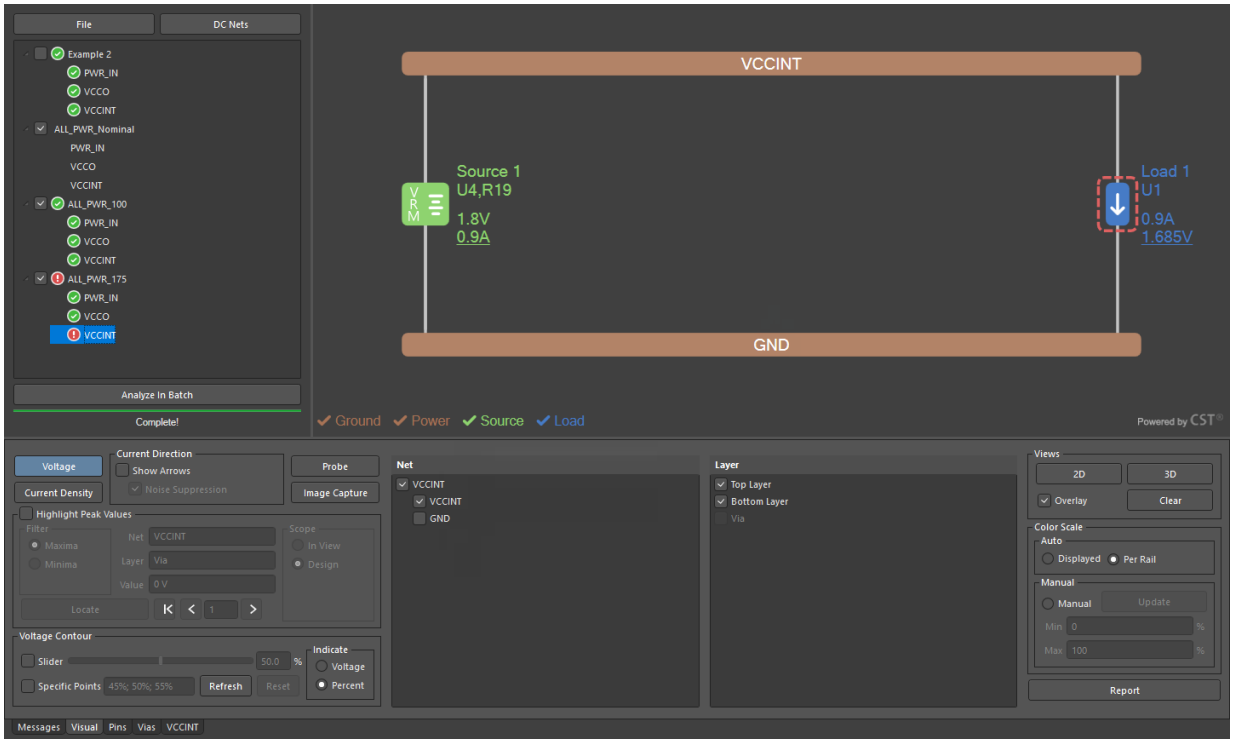
1. Select **File >> Open** and load configuration files: **ALL_PWR_100.pdna** and **ALL_PWR_175.pdna**.
2. Check the box next to the **ALL_PWR_100** and **ALL_PWR_175** network named within the panel.

Note: Doing so changes the **Analyze** button to **Analyze In Batch** as multiple configurations have been selected to run.

3. Now click the **Analyze In Batch** button to simulate the two newly added configurations files.

Note: It will take a few minutes for both new simulations to complete.

4. Successively click the voltage rail names within each network to view **Voltage Drop** and **Current Density** results.



PDN Batch Analysis

You can restart and load configurations to instantly view any existing simulation results stored in the active PCB project folder, even after exiting Altium Designer. In this guide, a maximum current limit check violation was identified on net **VCCINT** and corrected in the **ALL_PWR_Nominal** configuration. This configuration represented an ambient temperature setting of 25 degrees celsius.

The second configuration **ALL_PWR_100** represented an ambient temperature setting of 100 degrees celsius and resulted in no limit checks. The third configuration **ALL_PWR_175** represented an ambient temperature setting of 175 degrees celsius and resulted in a minimum voltage limit check at the load component on net **VCCINT**.

This new corner case error is the result of higher resistance in the copper as a direct result of increased ambient temperature. The existing copper traces are not adequate for operating over 150 degrees celsius, but could be modified to operate at 175 degrees. Subsequent modifications to the PCB and analysis of the **ALL_PWR_175** configuration could be performed to help achieve this requirement.

CONCLUSION

You made it to the end of the guide! Thank you for your attention. The guide provided just a quick snapshot at the key functionality of PDN Analyzer. Check out other **Getting Started** guides for insight into using robust features like **Draftsman®** and **ActiveRoute®**.

Remember to visit Altium.com/documentation to find other useful documentation, and learn about the latest in PCB design at the Altium Blog. If you want a more in-depth training experience, visit our Events page for online and in-person instructor-led training.