Altium®

Migration Guide

Migrating from Mentor PADS to Altium Designer®

TABLE OF CONTENTS

THE ALTIUM DESIGNER PHILOSOPHY

At the core of Altium Designer® is one central theme - a unified approach to PCB design. You'll find that our tool differs from many conventional alternatives in its approach to design. Our workflow unifies all of the separate yet connected elements required to successfully complete a PCB design.

As an existing PADS user, you are likely used to having multiple tools and interfaces for each stage of your design process. And while each tool excels in its own specialized task, at the end of the day you're left to manage and remember multiple interfaces, workflows, and methodologies. The question we've asked throughout the years is simple - is this approach to PCB design effective?

When we first created Altium Designer, we wanted to create a unified design experience that kept the engineer in complete control of their efficiency and workflow throughout the entire design process. Achieving this goal required us to understand what a complete PCB design experience entailed for the everyday engineer. As part of the unified approach to PCB design, we connected the following processes into one interface in Altium Designer:

- Schematic Capture
- Board Layout
- Data Management
- Rules and Constraints
- Bill of Materials
- Supply Chain Integration
- Engineering Change Management
- MCAD Collaboration
- Manufacturing Documentation Outputs

With all of these elements integrated in a unified interface, switching back-and-forth between tasks is as simple as selecting the appropriate file to work on in your design workspace. The unified interface then handles all the rest and provides the tools you need for the particular task at hand.

From our more than 30 years of PCB design research and development, we have found that a unified approach to PCB design is the most efficient way to design electronics. This philosophy extends not just to the individual engineer, but also to an entire design team. Projects can easily be worked on by multiple engineers in the same interface, and no time is wasted translating design data back and forth between design environments.

While many have labeled our approach to PCB design the "Altium Way," we consider it to be the best way to design advanced electronics right the first time.

We hope you enjoy your journey into the world of Altium Designer.

David Cousineau,
Sr Field Applications Engineer & The Altium Designer Team

PREPARING YOUR PADS FILES

IMPORTER INSTALLATION

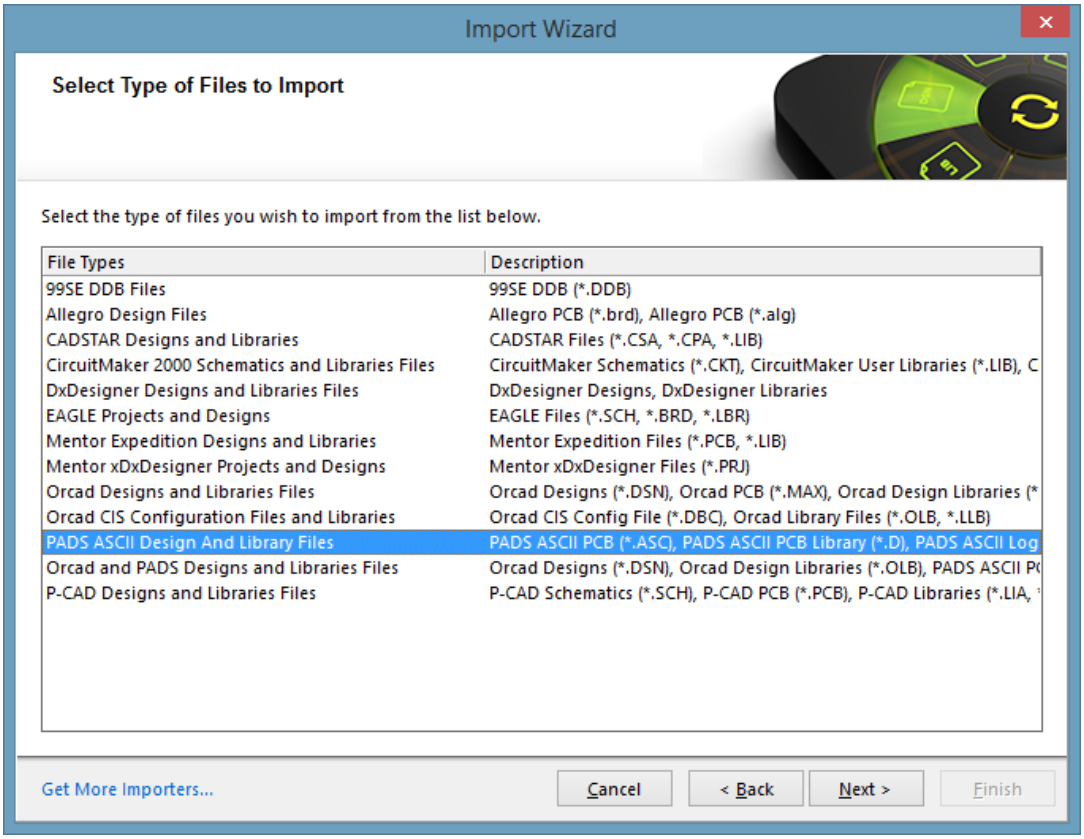
Before starting any PADS file preparation, the first step is to make sure the PADS Importer has been installed. This can be done directly from within Altium Designer. Follow the steps below to complete this:

1. Open Altium Designer.

2. Select **File » Import Wizard**.

3. Select **Next** on the Welcome screen.

The next screen, "Select Type of Files to Import," lists the installed importers.

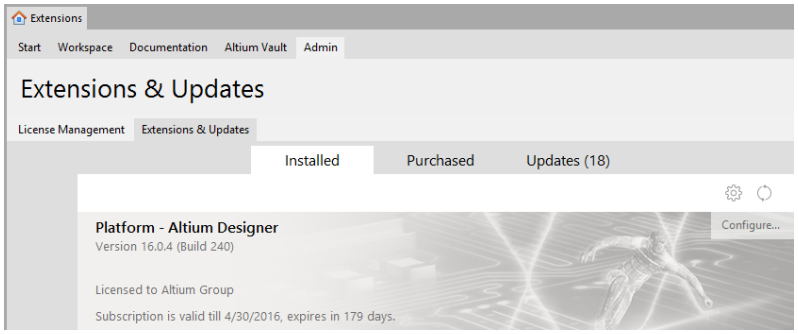


Altium Designer Import Wizard file type selection

During the installation of Altium Designer, you can choose which Importers and Exporters to install. By default, the PADS translator is not selected for installation.

If the 'PADS ASCII Design and Library Files' entry is missing from the list as shown above, then it must be added by following the steps below:

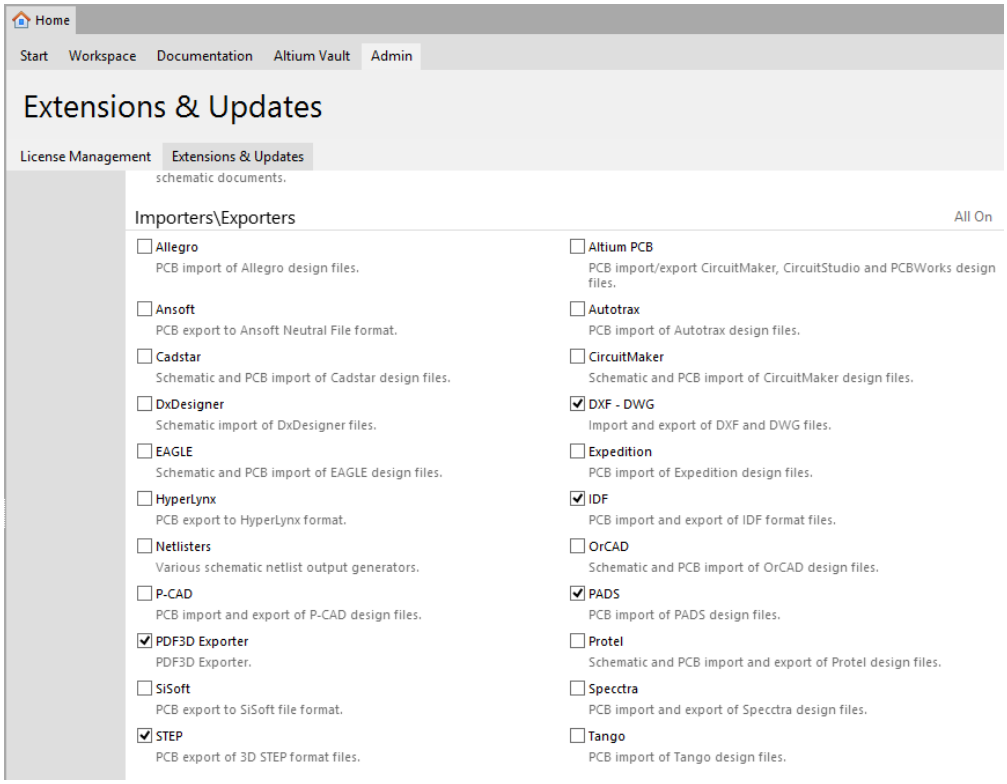
1. Select **Get More Importers...** at the bottom-left corner of the Import Wizard dialog window. This will open the Extensions & Updates tab inside the Altium Designer environment.



Altium Designer Extensions & Updates section

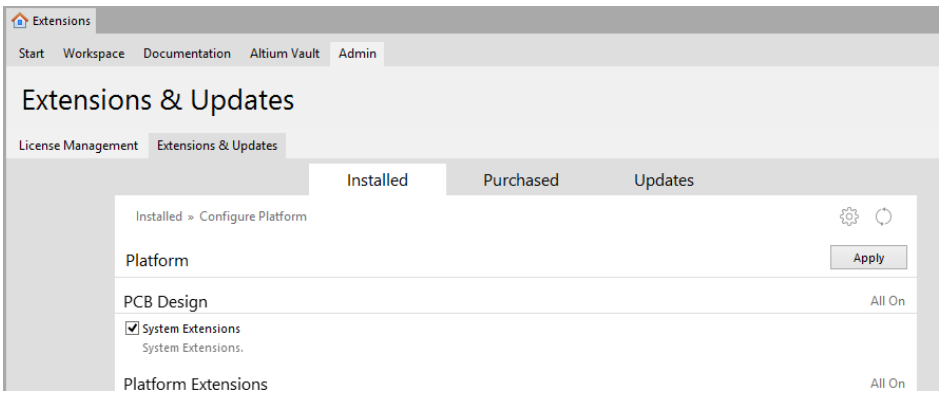
2. Select **Configure** on the right, scroll down to the Importers\Exporters section.

3. Select the checkbox next to PADS to enable the extension.



Enable the PADS importer in the Altium Designer Extensions & Updates section

4. Scroll back to the top and select **Apply** to complete the installation (Altium Designer will need to be restarted).



Altium Designer Extensions & Updates section

5. Select **File » Import Wizard** and confirm the PADS Importer has been added.

With the importer added in Altium Designer, you are now ready to start preparing your PADS files for the import process.

SUPPORTED PADS VERSIONS & FILE FORMATS

The PADS Import Wizard for Altium Designer supports a variety of file versions. It is recommended to use the latest PADS file version available as listed below.

- **PADS Logic/PowerLogic** – V5.2, V2005.x, V9.x, VX.1, VX.2
- **PADS Layout/PowerPCB** – V5.0, V2005.x, V2007.x, V9.x, VX.1, VX.2

Please keep the following things in mind when using the Import Wizard:

- The Import Wizard will translate schematics, PCBs, and library files.
- The wizard requires ASCII text versions of all file types in order to operate.
- The source PADS binary files (e.g. '*.pcb' for board files) may not be used as an import source.

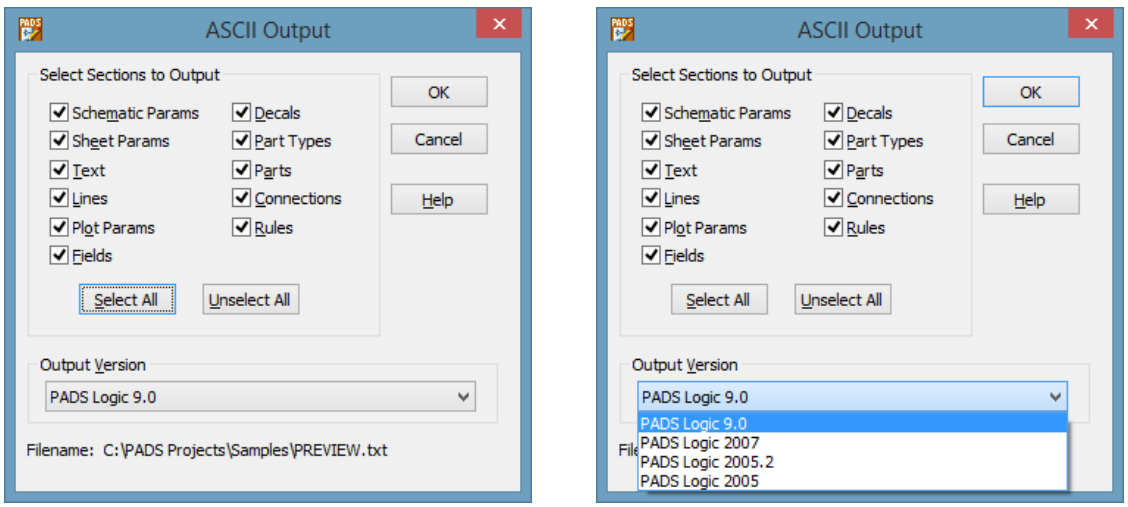
Unless the archived ASCII versions of the files are available, a valid PADS license may be needed in order to first create the necessary files. Details on each editor's ASCII creation process is outlined below.

ASCII FILE CREATION

PADS LOGIC

Schematics must be exported as an ASCII-based '.txt' file. This can be done with the steps below:

1. Open your schematic design in PADS Logic.
2. Select **File » Export**.
3. Change the file name and/or folder path if desired and select **Save**.
4. In the next dialog, select the **Select All** button to include all of your schematic data.
5. Select your desired output version in the Output Version drop-down box.
6. Select **OK** to create the file.

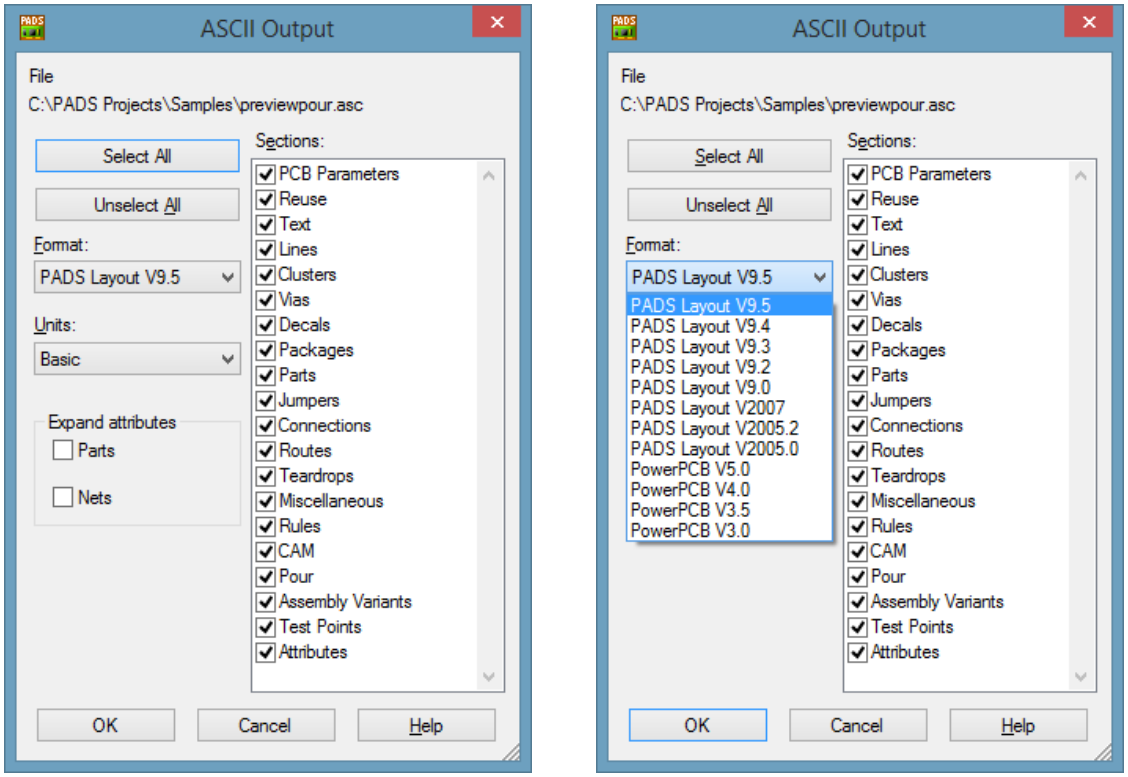


Creating an ASCII file for a schematic in PADS Logic

PADS LAYOUT

Designs must similarly be exported as an ASCII-based file ('.asc'). This can be done with the steps below:

1. Open your board layout in PADS Layout.
2. Select **File » Export**.
3. If desired change the file name and/or folder path and select **Save**.
4. Select your desired output version in the Output Version drop-down box.
5. Die gewünschte Version für die Ausgabe im Drop-Down menü auswählen.
6. Make sure the Units setting is set to **Basic**.
7. Select **OK** to create the file.



Creating an ASCII file for a board layout in PADS Layout

The Physical Design Reuse blocks in PADS cannot be translated. If these exist in the PADS design, they must first be broken apart into their base objects. This can be done in PADS Layout by selecting the Reuse block(s) and choosing Break Reuse in the rightmouse button menu.

PADS LOGIC SCHEMATIC SYMBOL LIBRARY

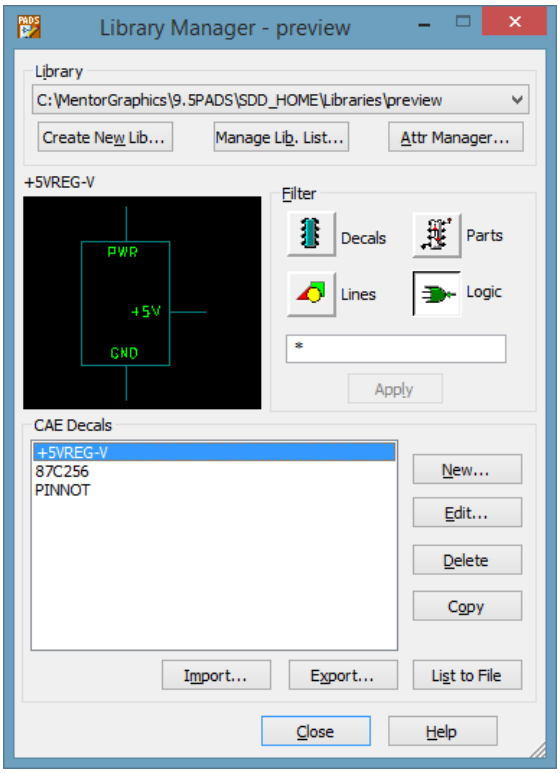
To translate a ***PADS Logic schematic symbol library***, it is necessary to export two ASCIIbased files from PADS. A PADS schematic symbol is comprised of two parts – the data from the CAE or Logic section (which is essentially the graphical representation of a part), and the data from Parts section (this area holds the parametric "intelligence" of the part).

The PADS library structure saves these sections with a '.ld9' extension for the CAE decals, and a '.pt9' extension for the parts. These are the source binary files and must be saved as ASCII for the translation process.
The corresponding ASCII file names are:

- *.ld9* (binary): *.c* (ASCII)
- *.pt9* (binary): *.p* (ASCII)

To export the libraries to ASCII format follow the steps below:

1. Open PADS Logic.
2. Select **File » Library** to launch the Library Manager.



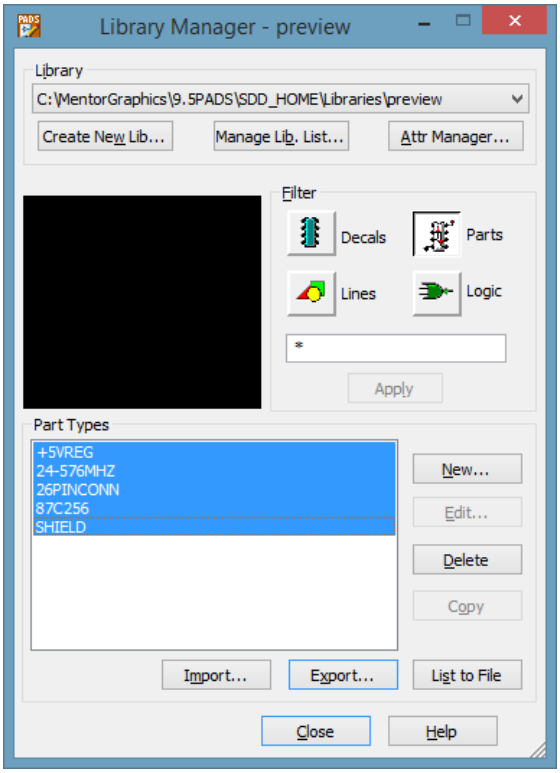
PADS Logic Library Manager

3. Set the Library filter to target a specific library (the All Libraries setting cannot be used for exporting).
4. Set the Filter to **Logic** to choose the CAE section of the library.
5. In the 'CAE Decals' list, select any or all of the decals to be exported.

TIP: to select the whole list, click the first entry, then scroll down and **Shift+Click** the last entry.

6. Now select the **Export** button to create a file with *a ".c"* extension.
7. Without leaving the Library Manager dialog, change the Filter to **Parts** and repeat the process of selecting the desired parts and exporting the file with *a ".p"* extension.

Please Note: When naming the *".c"* and *".p"* files, make sure that they share the same base file name. For example, for the library shown here, the files are *"preview.c"* and *"preview.p"*.



Selecting part types in the PADS Logic Library Manager

During translation, the Import Wizard will combine the graphical data from the *'.c'* file with the pin, attribute, etc. data from the *'.p'* file to create a single Altium Designer schematic library file with the extension *'.SchLib'*. More detail below in the "Translating Your Component Libraries" section.

PADS PCB DECAL LIBRARY

The ***PADS PCB Decal*** (or footprint) requires only one file type to export, as there is a one-to-one correspondence between the PADS decal library and the Altium Designer footprint library. The PADS library structure saves the decals with a '.pd9' extension. This is the source binary file and must be saved as ASCII for the translation process. The corresponding ASCII file name is:

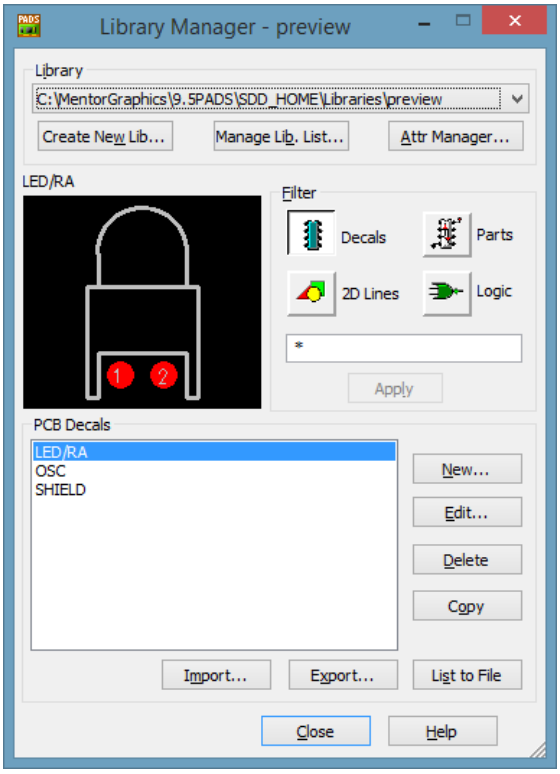
- *.pd9* (binary): *.d* (ASCII)

To export the PADS PCB Decal or footprint section follow the steps below:

1. Select **File » Export** in PADS Layout.
2. Set the Library filter to target a specific library (the All Libraries setting cannot be used for exporting).
3. Set the Filter to **Decals** to choose the PCB decals section of the library.
4. In the PCB Decals list, select any or all of the decals to be exported .

TIP: to select the whole list, click the first entry, then scroll down and **Shift+Click** the last entry.

5. Select the **Export** button to create a file with a *".d"* extension.



Select PCB Decals in the PADS Logic Library Manager

The *'.d'* file alone will be used by the Import Wizard to create an Altium Designer footprint library with the extension *".PcbLib"*.

Please Note: The 2D Lines section *('.ln9')* of the PADS library structure does not need to be exported, as it cannot be directly translated. Altium Designer does not store 2D drawing items in the library structure the way PADS does, so there is no corresponding or equivalent library file. If 2D items must be translated, then each individual item would need to be added to a PADS schematic or PCB, and then translated.

DATA INTEGRITY

It is important to remember that a translator is only as good as the source data allows. It is not uncommon for the source data in a PADS file to become corrupted.

If this is the case, it may not be evident to that file's use inside the PADS tools. However, when that data is exported to ASCII, as is required for this process, any anomalies in the formatting of the information can cause the importer to fail. This is by far, the biggest cause of translation failures. If this occurs, PADS has a relatively simple check to determine if the source data is corrupt.

To check if your source data is corrupt, you'll need to re-import the ASCII-based data to an empty workspace in the PADS editor where the data came from. Upon import, PADS attempts to reconstruct the file from the ASCII, and if it comes across anything "out of the ordinary" it gets thrown away and an error is logged.

This process is well-known among PADS users as "ASCII-ing in". For example, after creating the *'.asc'* from a PADS Layout design, select **File » New** to create an empty design file. Then select **File » Import** and open the newly-created *'.asc'* file.

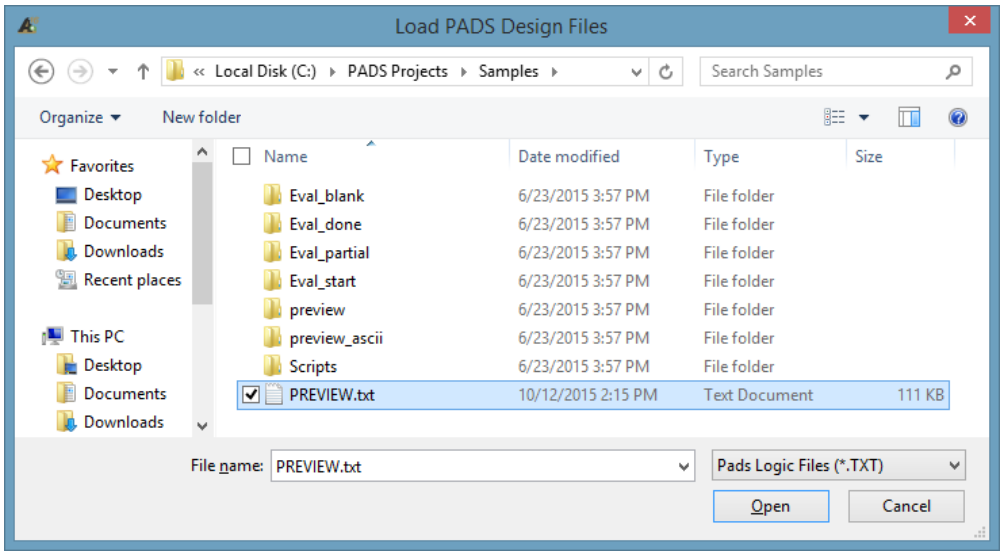
If there are no errors in the ASCII file, the PCB should appear as it originally did. However, if there are issues then those will get logged in the Output Window at the bottom of the PADS environment, and an error log written for further examination. Only when any PADS related issues are corrected can a new ASCII file get created for use with the Import Wizard.

TRANSLATING YOUR SCHEMATICS

SCHEMATIC IMPORTING PROCESS

The actual process of importing a PADS Logic schematic is simple and straightforward. Follow the steps below to complete this process:

1. In Altium Designer, launch the Import Wizard by selecting **File » Import Wizard**.
2. Select **Next** on the welcome screen.
3. Select the "PADS ASCII Design and Library Files" entry under File Types and then **Next** to continue.
4. Select **Add** to load a PADS design file (The default setting for this screen is to look for PADS Layout files with the '.asc' extension).
5. Change the drop-down in the bottom right to "PADS Logic Files ('*.txt') and then browse to the location of the exported PADS Logic file.



Loading PADS design files from the Altium Designer Import Wizard

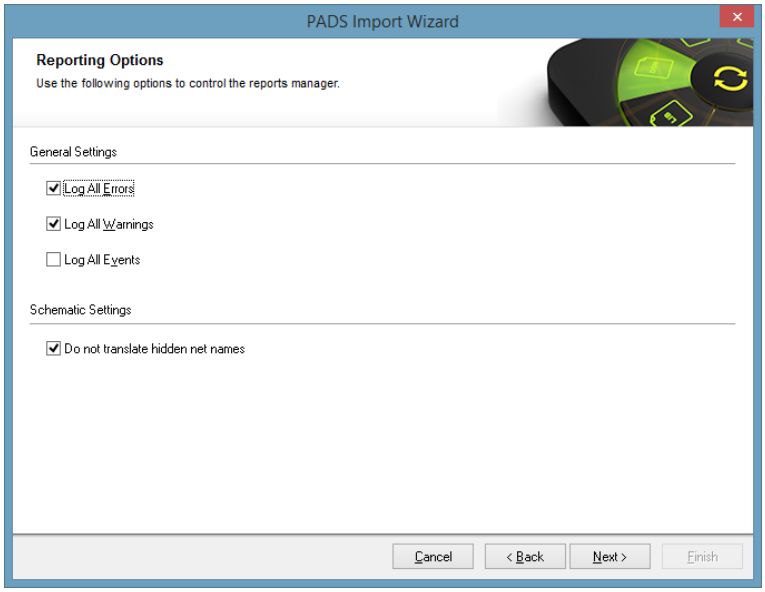
Multiple files can be selected in this dialog and added for translation. If the files are across different folders, select the Add button again and browse to a different location to add more files.

Please Note: It is also possible to translate PADS Logic files and PADS Layout files in the same session. To do this just select **Add** den Dateityp für Layout-Dateien auf „PADS Design Files (*.asc)" ändern.

6. Select **Next** to continue through the Import Wizard.
7. On the Reporting Options screen, it is recommended that '**Do not translate hidden net names**' be enabled.

Please Note: Every schematic software system has a way of assigning net names for non-user defined net names (i.e., those nets that aren't given a specific name like *CLK* or *GND*). PADS Logic handles these system generated net names with a name starting with "$$$" and then a randomly generated number sequence (e.g., *$$$16581*).

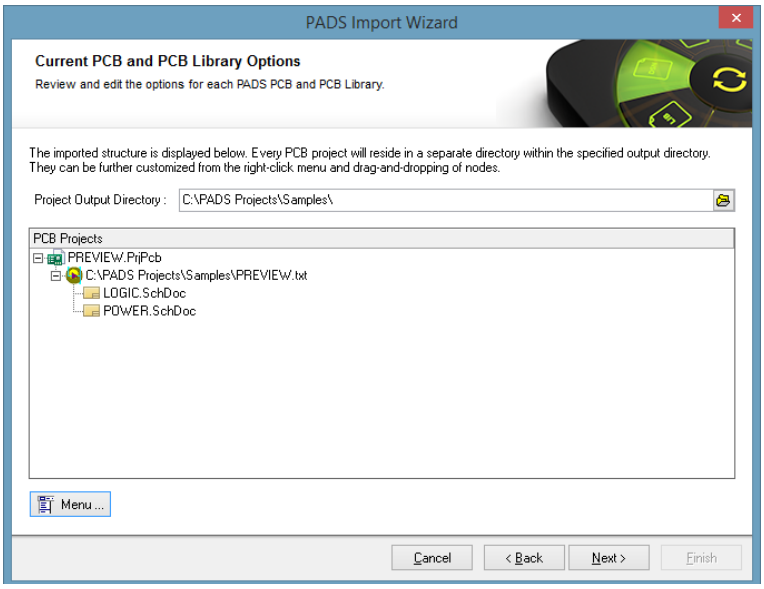
Altium Designer auto-generates net names differently (a prefix of "Net" followed by the pin number of a connected component – *NetC1_1*), and it is better to allow Altium Designer to maintain its own record of these non-labeled nets. The biggest drawback is that if these "$$$" net labels are brought over to Altium Designer, they would be visible on the schematic page which can be visually distracting and can even cause some connectivity errors.



Configuring Report Options in the PADS Import Wizard

8. Click **Next** to get to the review page which will present a summary of what is being translated and where the files will be saved.
9. The 'Project Output Directory' defaults to the location of the selected file(s), or will be blank if multiple folder locations were used.

Please Note: The results of the translation (i.e., the created Altium Designer files) will be placed in a new folder underneath the Output Directory, thus it is not necessary to create a folder for the translated data.



Selecting the Project Output Directory in the PADS Import Wizard

10. Click **Next** at this point will start the translation process. The number and size of the designs will determine the length of time needed to complete the translation – anywhere from just a few seconds for small designs up to several minutes for very large ones. The "complete" screen will appear when the process is done. Click **Finish** to close it and review the translated schematic(s).

SCHEMATIC CLEANUP

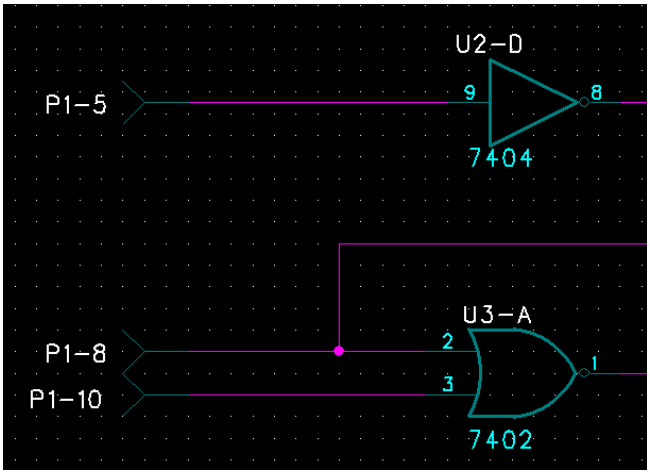
There will always be at least a little bit of cleanup work to do. This is usually due to incompatibilities between the two CAD systems' data structures, or just differences in how certain features or object types were implemented.

This section will address the common areas of the translated schematic that should be inspected. The assumption for this and subsequent cleanup sections is that the user has at least a basic understanding on the use of Altium Designer. To learn the basics of Altium Designer, please view Exploring Altium Designer.

Connectors

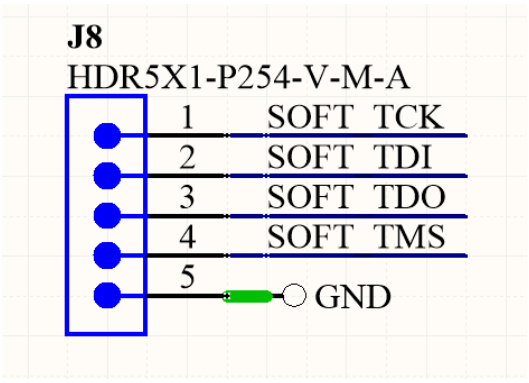
One of the main differences between PADS Logic and Altium Designer is the support for connector components. Logic has a special type of connector component type which allows the individual pins of the connector to be placed and moved about individually.

Altium Designer does not support this and treats connectors as it does any other type of component in which all of the pins are grouped together as a block. Below is an example of a Logic schematic with the pins of connector P1 placed individually.



Example of a connector in PADS Logic

By comparison, a typical Altium Designer connector keeps the pins together in a block as shown below:



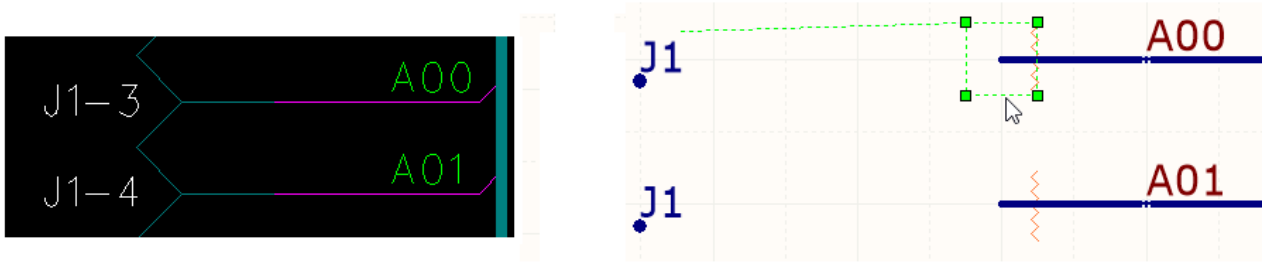
Example of a connector in Altium Designer

Because of this incompatibility, any connectors that are created this way in PADS Logic will need to be replaced with an Altium Designer "block-style" connector. This can be done pre- or post-translation and may mean some major changes in the layout of the schematic.

Removing Translated Connectors in Altium Designer

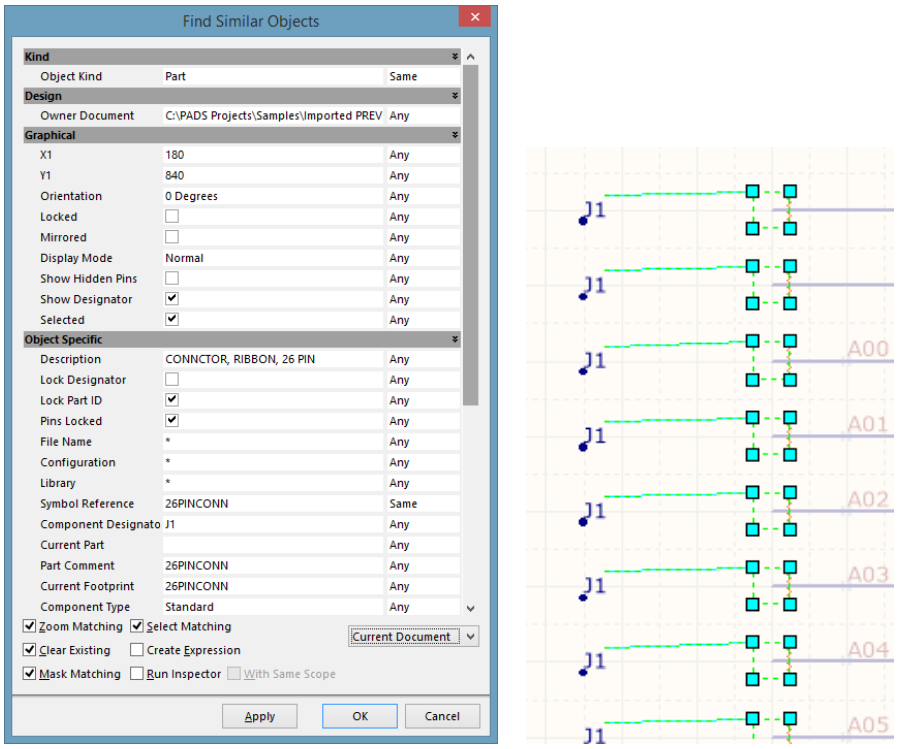
To quickly remove translated connectors in Altium Designer with the Find Similar Objects feature, follow the steps below:

1. First find one of the connector locations. Because this object type is not supported, no graphical conversion is actually made.
2. Select the spot where the connector pin should be and the "ghost" part will be selected and highlighted as shown below:



Selecting connector pins in Altium Designer

3. Right-click inside the selection box and choose **Find Similar Objects** from the pop-up menu.
4. Scroll down to the 'Symbol Reference' field and change the drop-down dialog from **Any** to **Same**.
5. Make sure that the **Select Matching** checkbox at the bottom of the dialog is enabled and select **OK**.
6. With all of the connector pins now selected, a simple press of the **Delete** key will remove them all from this page. Repeat the process for each schematic sheet.



Using the Find Similar Objects feature in Altium Designer

For more information on the Find Similar Objects feature please see the following Altium Designer documentation articles:

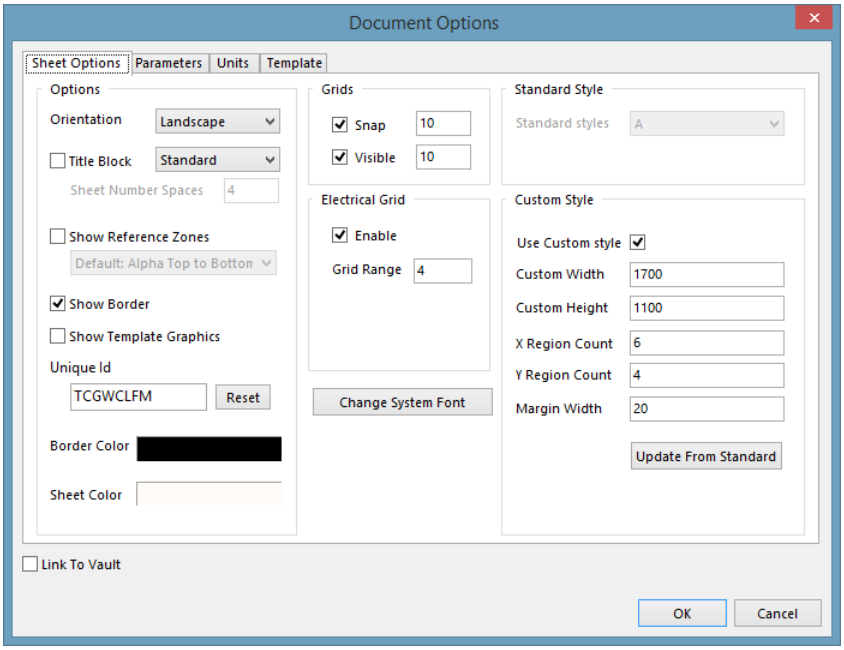
- Editing multiple objects in Altium Designer
- Finding similar objects in Altium Designer

Schematic Borders/Templates

While Altium Designer supports reusable schematic sheet templates, the schematic sheet border and title block areas in PADS Logic are little more than combined lines, text and graphics and thus are indistinguishable from other 2D objects. Therefore, this data is brought over in its raw form as lines and text. Any embedded graphical objects such as logos are not translated.

Altium Designer will automatically display its own sheet border and title block, so there may appear to be duplicated info. It is left to the user to decide whether to keep the translated border, or to replace it with an Altium Designer template. To quickly disable the display of the Altium border follow the steps below:

1. Select **Design » Document Options**.
2. Within the *Sheet Options* tab, disable the **Title Block** and **Show Reference Zones** checkboxes as shown below.
3. To remove the translated border, several methods could be used to select and delete the data. For example, 'Find Similar Objects' or the selection commands in the **Edit » Select** menu (particularly **Select Outside Area**).



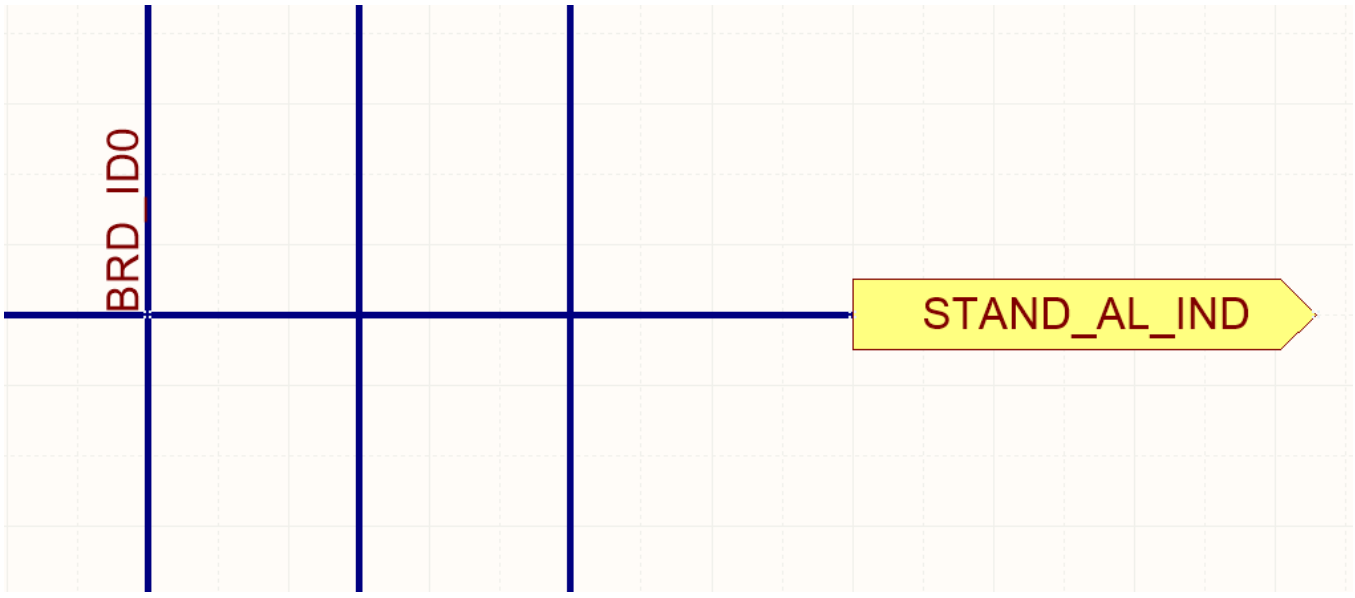
Configuring Document Options in Altium Designer

Net Labels

Another major difference between Altium Designer and PADS Logic is the way in which nets are named. PADS Logic allows for a wire or connection to have a property embedded in it to indicate the name of the net (e.g., CLK). That net name can then be displayed on the schematic or hidden from view.

Altium Designer uses a different method whereby a special type of string called a "Net Label" is physically placed on the wire or connection. If a net name exists in PADS Logic and is then brought over to Altium Designer, that net label will be placed at the midpoint of its respected wire.

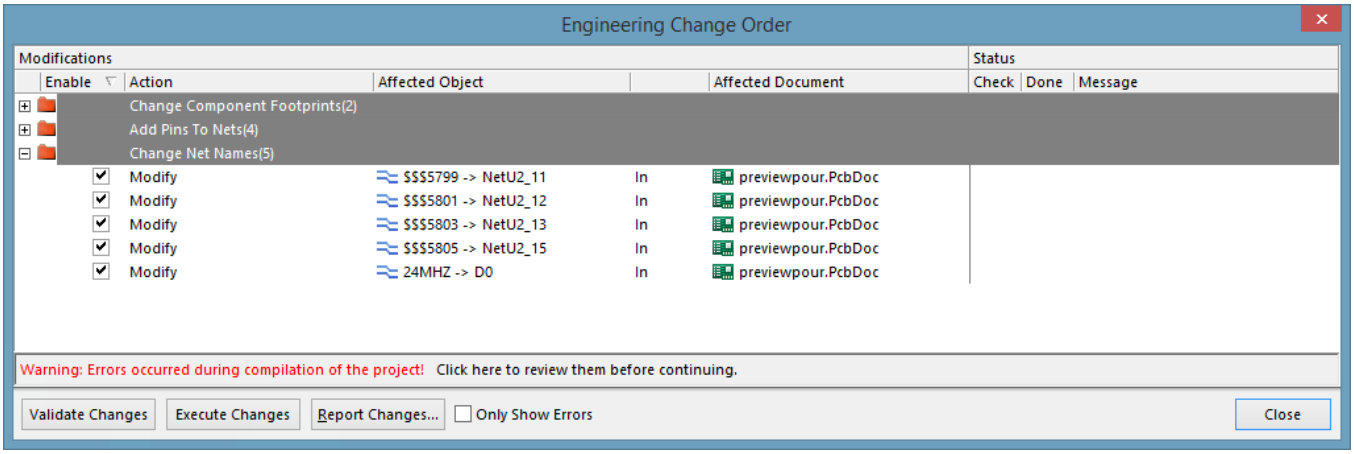
One very rare, but possible, situation is when the midpoint of a wire segment exactly intersects another wire, the net label will be placed at that intersection point and effectively name ***both*** wires.



Net label placed at the intersection point of two wires

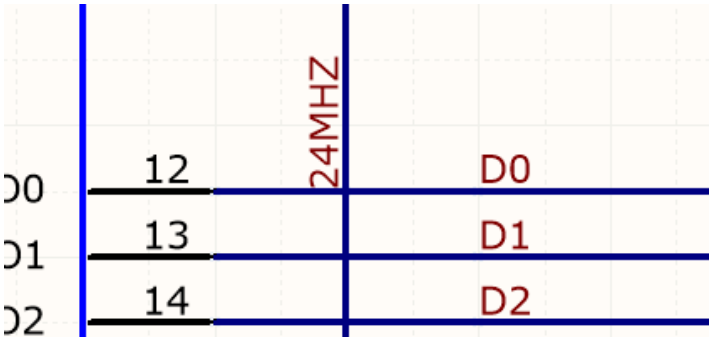
In this example, The BRD_ID0 label is connected to the vertical wire, but also to the horizontal wire connected to the STAND_AL_IND port. The STAND_AL_IND net will be renamed to BRD_ID0 in this case. Obviously this is not desirable.

One way to locate this issue is by a visual inspection of the design. A better approach relies on there being a corresponding PCB design that has also been translated from PADS Layout to Altium Designer. Once the schematic and PCB are synchronized, running an ECO will show when the system attempts to rename a net. This is a good indication that there is a connectivity issue in the schematic, that was not intended in the original design



Running an ECO to check for connectivity issues in a schematic

In the above example, the 4 nets prefixed with $$$ are the system-assigned net names being changed from the Logic-named format to the Altium Designer-named format, which is what we want. However, the *24MHZ* net being renamed to D0 is not an intended change, and needs to be investigated further.



Conflicting net labels in Altium Designer

After we cross probe to the schematic design, we find that the *24MHZ* net is placed on both its own wire and a wire labeled *D0*, creating a conflict that needs to be resolved by moving the *24MHZ* net label away from the D0 wire.

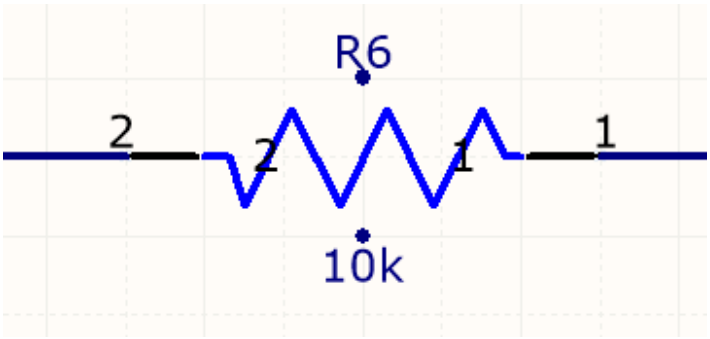
Manually Placed Parameters

Visible component parameters in Altium Designer are usually set as 'autopositioned'. This means that the system will place the parameter – including a reference designator – in a default location alongside the symbol body. This is helpful when rotating components, as the system will place the parameters in a neat and readable position.

In an effort to exactly duplicate the source schematic from PADS Logic, imported parameters have their auto position setting disabled. The reference designators and parameters are then placed as close to their original position as possible, and are now considered 'manual parameters'.

Because of differences in default text styles and sizes an exact match may not always be possible. The user may want to slightly change the parameter text positioning.

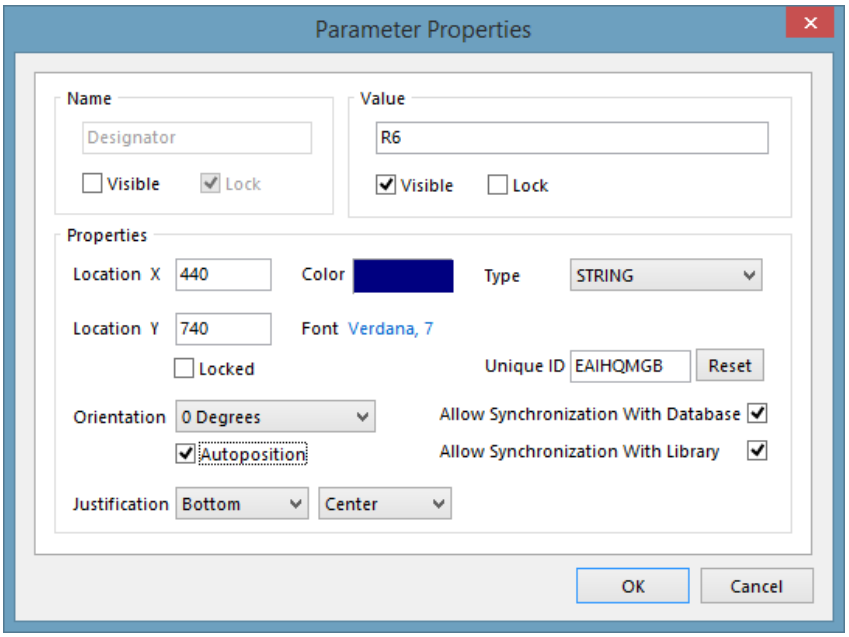
Parameters that are 'manually positioned' are marked with a small dot as shown below:



Manually positioned parameters on a schematic symbol

You can choose to handle with these 'manual parameters' in one of three ways:

- Leave the design as-is.
- Leave the parameters where they are but turn off the dot. This can be done by selecting **Tools » Schematic Preferences** then selecting the **Graphical Editing** group, and disabling the **Mark Manual Parameters** option.
- Re-enable the 'Autoposition' setting in the *Parameter Properties* dialog as shownbelow. This can be done by using a combination of 'Find Similar Objects' and the 'SCH Inspector' panel.



Editing Parameter Properties in Altium Designer

Because the autoposition of parameters is only done during component placement or the rotation process, the effect of the auto position won't be seen until the components are rotated in place.

To rotate all components in place:

1. Press **Ctrl+A** to select everything on the schematic sheet

2. Press **Spacebar** to rotate everything 90 degrees
3. Press **Shift+Spacebar** to rotate everything back to the original positions

All parameters and designators will now be positioned automatically.

Connectivity Differences

There are many other subtle differences between PADS Logic and Altium Designer in allowable connectivity structures. Altium Designer supports true hierarchy, where the sheet-to-sheet connectivity can traverse both vertically and horizontally, while PADS Logic does not support any of these complex schematic structures.

Connectivity problems may become evident after running the Project Compile process (**Project » Compile PCB Project**). The Messages panel will report these errors and warnings indicating these hierarchical and net connectivity mismatches. For instance, a "Duplicate net names" error usually points to improper sheet-to-sheet connectivity.

Rather than address every possible situation here, a good exercise is to become familiar with is Connectivity and Multi-Sheet Design within the TechDocs.

Inverted Signals

PADS Logic and Altium Designer have slightly different methods of indicating an inverted signal. PADS uses the "\" (backslash) character to indicate that all characters after the slash are to show a bar. An inverted INIT signal would therefore be created by giving it the net name \INIT which would appear in the schematic as shown below:

Inverted signals in PADS Logic

Altium Designer supports two methodologies for signal inversion or negation. If the "\" character is used as the first character in a net label ***AND*** the schematic preference **Single ' \ ' Negation** is enabled (**Tools » Schematic Preferences » Schematic » Graphical Editing**), then the *\INIT* net will appear in the schematic as shown below:

Inverted signals in Altium Designer v1

The other Altium Designer method is to instead use the "\" character after the character that is to be inverted. A main difference here is that each character can be independently inverted. So the inverted "INIT" would be notated as *I\N\I\T*. It then allows a mixed situation such as *HIGHL\O\W*.

Inverted signals in Altium Designer v2

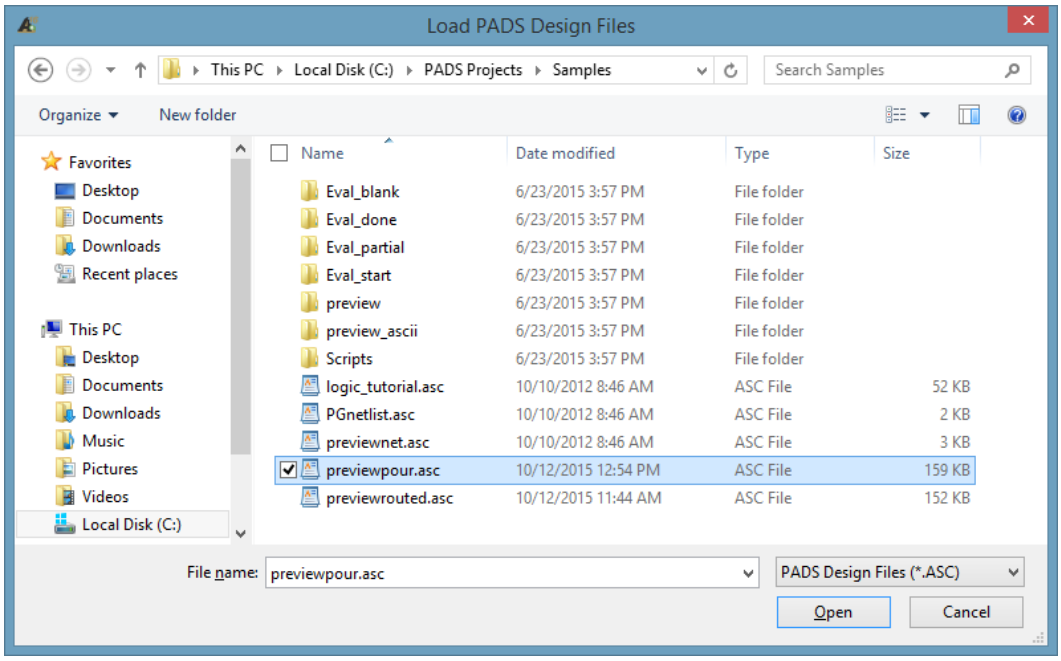
The same net name in PADS Logic would be created as *HIGH\LOW* (everything after the "\" is inverted). Since the single ' \' negation method used in Altium Designer requires that a user's preference be set (and different users can have different preference settings), it is generally safer to use the method of placing the backslash after the character(s) to be inverted. It is recommended that the schematic design be analyzed for inverted signals and their net labels be changed from the PADS single-backslash to the Altium Designer multi-backslash. There are several methods to locate these nets. One is to use **Edit » Find Text**. Another is to first Compile the Project, and then use the Navigator panel (**View » Workspace panels » Design Compiler » Navigator**). Sort the Net/Bus by name and the nets beginning with "\" will appear at the top or bottom of the list. The changes themselves will need to be made manually or via **Edit » Replace Text**.

TRANSLATING YOUR PCBS

THE PCB IMPORTING PROCESS

Translating a PADS Layout starts in the same way as a PADS Logic translation. Follow the steps below to complete this process:

1. Select **File » Import Wizard**.
2. Select **Next** on the welcome screen, choose PADS ASCII Design and Library Files and then select **Next** to continue.
3. Select **Add** to load one or more design files. The default file type is to '.asc' files.



Loading PADS Design Files in the Altium Import Wizard

WARNING: Be aware that PADS works with two file formats that share the ".ASC" extension. One is the export of the PCB file discussed previously and what is needed for this process. The other is the netlist – the file generated from the schematic used to populate the PCB design. This file format is NOT usable here. Both files are text based and can be opened in a text editor. The PCBexport ASCII file (correct) will begin with something similar to this:

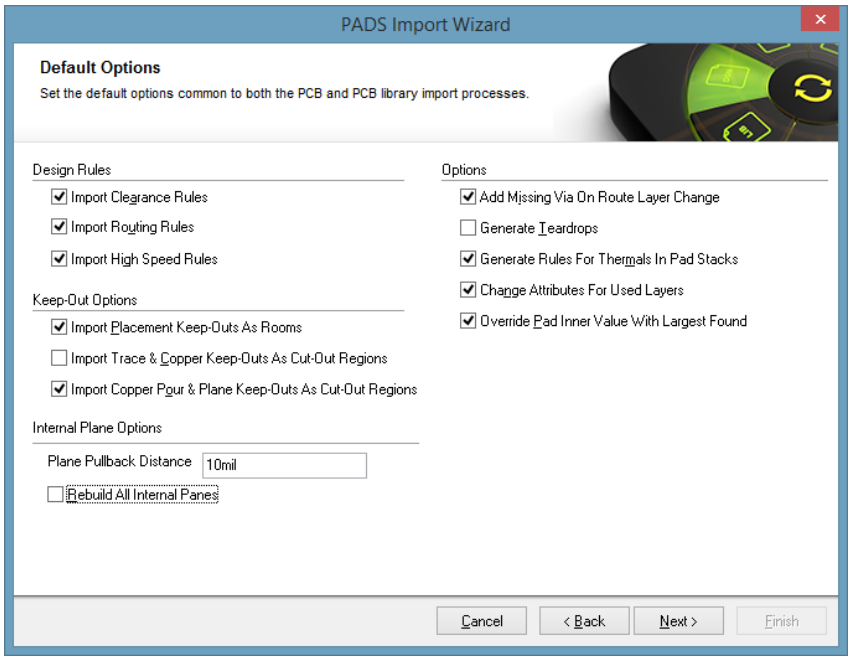
```
!PADS-POWERPCB-V9.5-BASIC! DESIGN DATABASE ASCII FILE 1.0
*PCB*      GENERAL PARAMETERS OF THE PCB DESIGN

UNITS      0          2=Inches 1=Metric 0=Mils
USERGRID   317373 317373  Space between USER grid points
MAXIMUMLAYER 4          Maximum routing layer
```

Whereas the netlist file (incorrect) will look like this:

```
!PADS-POWERPCB-V9.0-MILS! NETLIST FILE FROM PADS LOGIC V9.5
*REMARK*      PREVIEW.SCH      --      Thu      Oct      15      09:06:19      2015
*REMARK*
*PART*      ITEMS
U1      87C256@SO28
U2      87C256@SO28
```

4. Select **Next** to continue through the wizard. If library files are being translated, they can be added at the next screen.
5. The Reporting Options screen can be left as-is (assuming no schematics are being translated).
6. The Default Options screen may require some adjustments before continuing as explained below.



Laden von PADS Designdateien in den Altium Designer Import Wizard

- **Design Rules**: This section is self-explanatory. Should the Clearance, Routing, and High Speed rules be imported or not.
- **Keep-Out Options**: If these options are left unchecked (disabled) any PADS placement, trace/copper, and copper pour keepouts will be converted to an Altium Designer keepout area. There is a fairly major difference in the tools here, as PADS' keepouts are configurable as to the type of object they keep out, Altium Designer keepouts are global – meaning any electrical object (trace, via, pour, etc.) will be checked against the keepout for DRC violations.

Note:

Placement: The Altium Designer equivalent of a placement keepout uses a Room, so it is advisable to enable the Import Placement Keep-Outs As Rooms option.

Trace & Copper: The Altium Designer keepout operates much like the PADS trace & copper (not copper pour), so this option can usually remain off so a keepout.

Copper Pour & Plane: The Altium Designer pour and plane cut-outs are equivalent to those in PADS. It is safe to keep this option always enabled.

- **Internal Plane Options**: For layers that will get converted as negative plane layers, set the pull-back distance to the desired gap from the plane copper to the board edge. In PADS, this is manually done and involves either setting the Board Outline width to double the plane pull-back, or by drawing a line on the plane layer that matches the board shape. Altium Designer creates this pullback distance automatically, via a setting in the Layer Stack Manager dialog (**Design » Layer Stack Manager**). As the user you will need to understand how the design was created in order to determine what to set this value at.
- **Options**: The important option in this list is "Generate Teardrops." Enabling this option will automatically add teardrops to the design, whether they existed in the original PADS design or not. It is highly advisable that this option be disabled. If the source PADS design includes teardrops, then they will be removed as their structure is different than how Altium creates teardrops.

Layer Mapping Configuration

Continuing with the steps above for importing your PCBs, you'll now need to configure the layer mapping and finalize the import process with the steps below:

7. On the next screen, select the **Edit Mapping** button to analyze how layers are translated.

Efforts will be made to ensure, for instance, PADS silkscreen layers map to Altium silkscreen layers. Layer mapping can be manually adjusted if desired. In addition, PADS layers can be set to "Not Imported" if information from a particular layer can be discarded. It is not required to have all PADS layers mapped to an Altium layer.

Specific to internal layers, PADS inner signal (routing) layers will be mapped as Altium Designer Signal layers (e.g., "Mid Layer 1"). PADS CAM Plane layers will be mapped as Altium Designer Plane layers (e.g., "Internal Plane 1"), which are negative-image planes. PADS inner layers defined as split/mixed layers will be initialized as Altium Designer Signal layers if any trace or other positive-image electrical data is present.

If the split/mixed layer only has pour shapes it will be initialized as an Altium Designer Plane layer (negative), and imported with all split, embedded, and isolated plane area intact. This setting can be changed manually if you would prefer to import the split planes as positive layers.

If multiple files are being translated at the same time, each will have its own layer mapping choices, so be sure to examine each unique layer stack.

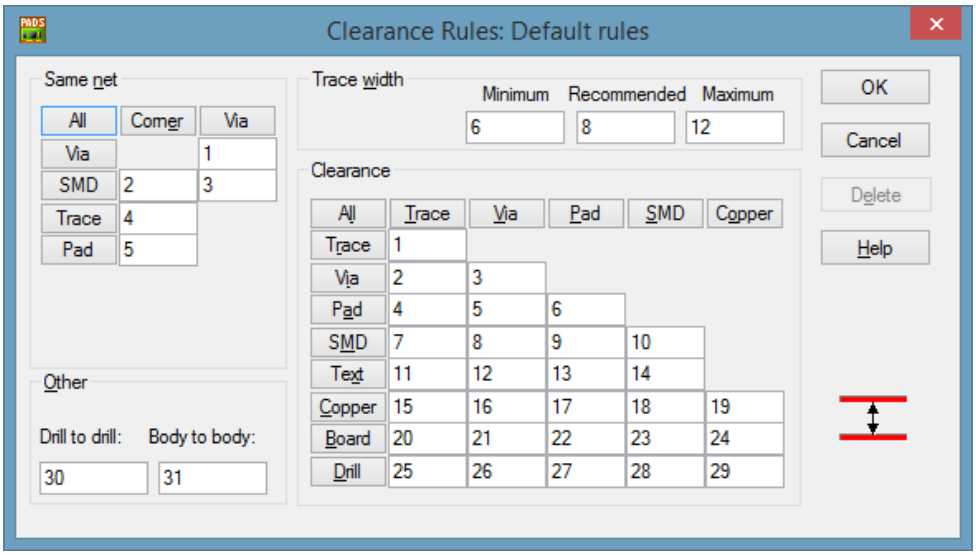
8. Select **Next** to go to the review page which will present a summary of what is being translated and where the files are saved.
9. The 'Project Output Directory' defaults to the location of the selected file(s), or will be blank if multiple folder locations were used.
10. Selecting **Next** will start the translation process. The number and size of the designs will determine the length of time needed to complete the translation – anywhere from just a few seconds for small designs up to several minutes for very large ones.
11. The "Complete" screen will appear when the process is done. Select **Finish** to close it and review the translated PCB file(s).

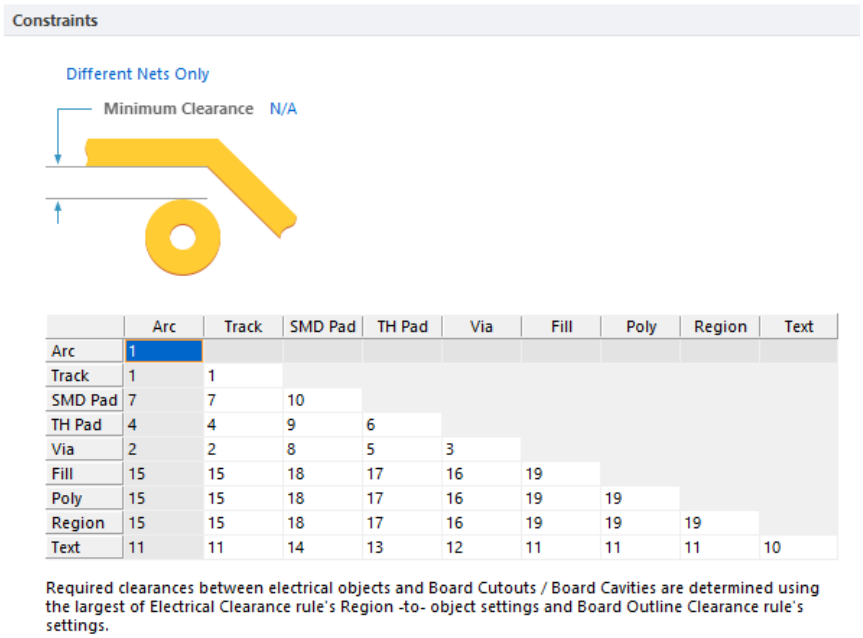
PCB DESIGN CLEANUP

Although the translator does an excellent job of accurately converting the PCB data, incompatibilities between the two CAD systems could result in the need for further editing to the imported design.

Design Rules

When it comes to basic clearance rule setup, PADS Layout and Altium Designer share a similar matrix-based methodology. For instance, a value set in the PADS via-to-via rule will be transferred to the Altium Designer via-to-via rule. As an example of how each clearance value will be converted, use the example below. For now, we will focus only on the main clearance matrix.





Clearance rules in Altium Designer

Notice that Altium Designer distinguishes between a routed arc and a straight portion of a route (termed a "track"). The clearance values for PADS traces are transferred to both tracks and arcs in Altium Designer. Also notice that PADS' single value for copper is used for fills, regions, and polygons (Altium Designer fills and regions are equivalent to PADS copper, while Poly, or Polygon, is the equivalent of PADS copper pour)

Missing from the Altium Designer clearance matrix are the “Board” clearance values. The Board Outline clearance setting is a different rule setup (specifically, in the Manufacturing design rules). At this time the board clearance values are not transferred to Altium Designer and must be created manually.

The drill-to-object values do not have exact equivalents in Altium Designer (e.g., a check cannot be made from a drill edge to an SMD pin). Instead, Altium Designer includes a hole-to-hole check as part of the Manufacturing design rules. The PADS global “drill-to-drill” value (30, in this example) ***is*** transferred to Altium Designer as a hole-to-hole rule.

TIPS: Specific hole-to-hole rules can also be created in Altium Designer, so a 30 mil drill can have a different clearance from other holes than a 20 mil drill, if necessary.

For the “Same Net” clearance rules, the via-based rules are recreated in Altium (via-via, via-SMD). However, Altium Designer does not have a “corner” object type, so those rules are not transferred.

PADS Conditional Rules like Net Classes, Nets, Differential Pairs, etc. are all transferred as expected.

There are no equivalent Altium Designer rule types for Pin-pairs, Pin-Pair Groups, Decals, or Components and will not be translated.

Keepouts

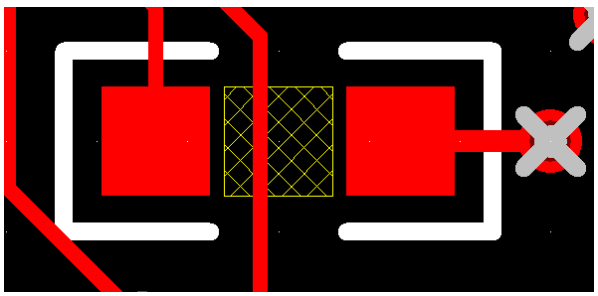
As discussed in the Import Process section, PADS keepout objects have different capabilities than Altium Designer. While a keepout in Altium Designer can be constrained to a specific layer and can have any physical shape, it will apply keepout to all electrical types – be it a via, trace, component pad, etc. By contrast, a PADS keepout can be configured to exclude specific object types (e.g., to keepout vias but not traces).

The *Import Wizard* does have a few controls to ensure one-to-one functionality for certain scenarios (Use ‘Import Placement Keep-Outs As Rooms’). However, care must be taken to understand the keepout types in the source design and how they may function in Altium Designer and affect the design rule checking.

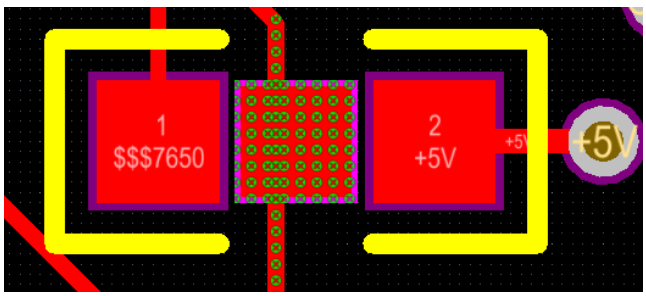
When a PADS keepout is configured to keep out more than one object type, only one keepout object will be created in Altium Designer. The type created will depend on which keepout options are set in PADS and how the Import Wizard Keepout options are enabled.

The keepout incompatibilities can also extend into PCB footprints. PADS PCB decals can contain the same configurable keepout objects. It is common for designers to include, for example, a keepout area between the PADS of an SMD capacitor, preventing vias from being placed between the pins although still allowing traces.

In the figure below, the footprint in Altium Designer will include the keepout region between the pins, but in addition to the keepout checking for vias, the keepout will flag an error for any electrical item (traces, copper pours, etc.). The PADS keepout may translate into an object that could produce unexpected DRC violations.



Footprint in PADS with a via keepout



Footprint in Altium Designer with keepout

These footprints will have to be edited in the Altium library to remove the keepout if this situation occurs.

Polygon (Copper) Pour Thermals

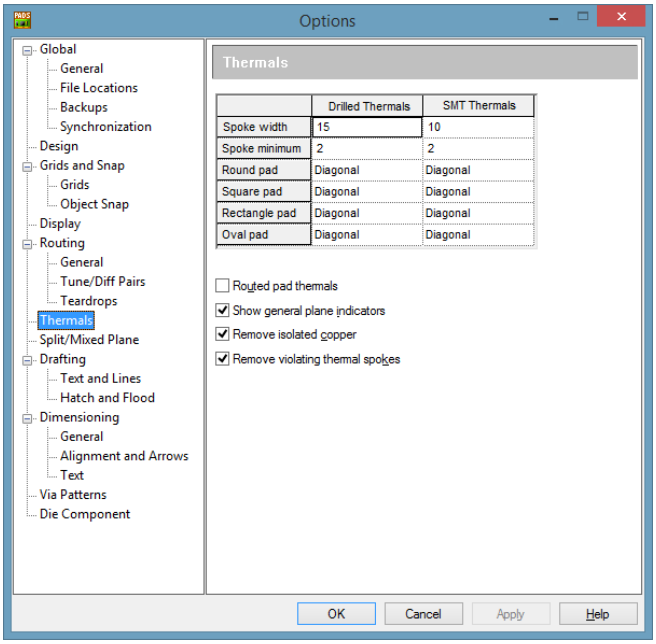
All PCB systems handle copper pour and thermal generation differently. PADS allows thermal connectivity to be defined in many ways, both globally and at the individual padstack level. Thermals can differ depending on the pad shape (45 degree connection on round pads vs. 90 degree connection on ovals), or be defined at the decal and even a single pin level. Via thermals can be defined per via style, and then overrides for floodovers can be set for individual copper pours. Design rule settings can also affect thermal connectivity. Lastly, CAM output settings can change how connections are made to (negative) CAM planes.

Altium Designer takes an altogether different approach to thermal generation by managing these settings in the design rules ('Polygon Connect Style rules'). In practice, this methodology allows for more efficient thermal setup, due to the fact that all of the settings concerning thermal connections are in one place.

In earlier versions of Altium Designer, the PADS Import Wizard attempted to recreate every conceivable thermal connection option that existed in the PADS design. The result was an unmanageable list of polygon connect design rules, ranging from just a handful of rules for very simple designs to literally hundreds of rules for more complex designs.

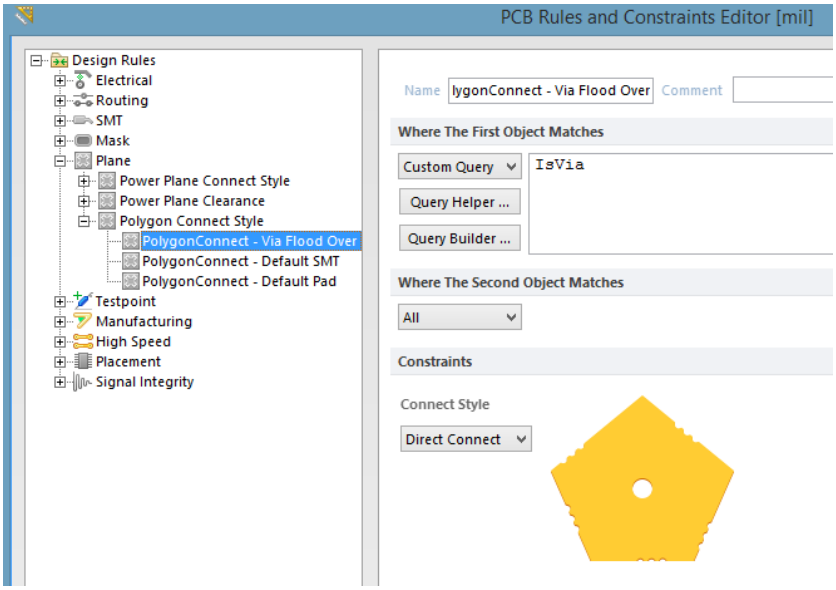
Post-translational cleanup and combining of the rules was always necessary, and most users decided to simply remove them all and recreate the polygon connect rules "the Altium Designer way." Usually the result was a short list of rules that addressed almost all, if not all, scenarios present in the source PADS design.

The decision was therefore made to remove attempts at recreating thermal connectivity with the exception of two Polygon Connect rules – one default connection for all pins and vias, and one specifically for SMT pins. The default rule will create a 4-spoke relief connection with the spoke width determined by the PADS spoke width for 'Drilled Thermals' in the **Options » Thermals** dialog:



Thermal options in PADS

The Altium Designer SMT connection rule will have its thermal spoke width determined by the 'SMT Thermals' spoke width setting in the PADS **Options » Thermals** dialog. If any other specific thermal connection configuration is needed, you will need to create these rules manually within Altium Designer. One common example is a rule that specifically targets vias for "flood over" connectivity. This is achieved by creating a new rule, and setting the Scope to "IsVia" vs. "All" and the Constraints to "Direct Connect." For more information on design rule creation, please refer to Constraining the Design - Design Rules within TechDocs.

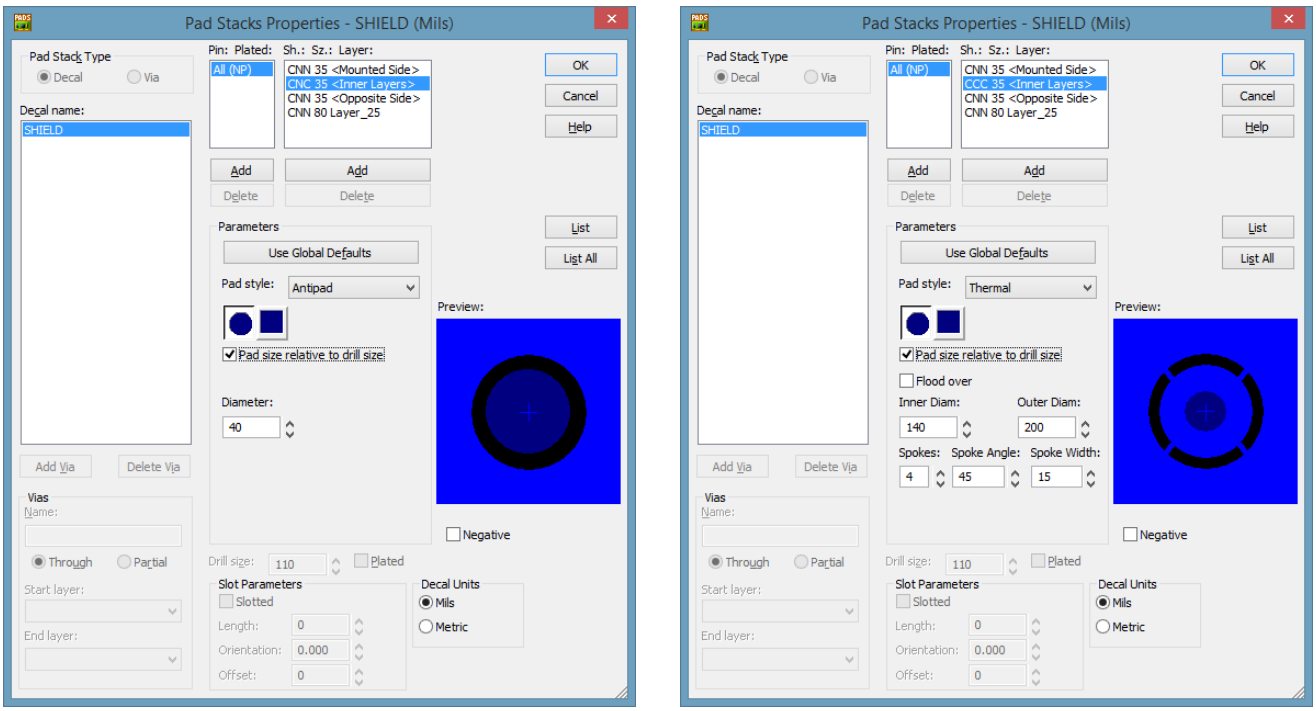


Configuring design rules in Altium Designer for polygon connectivity

Plane Thermals and Plane Clearances

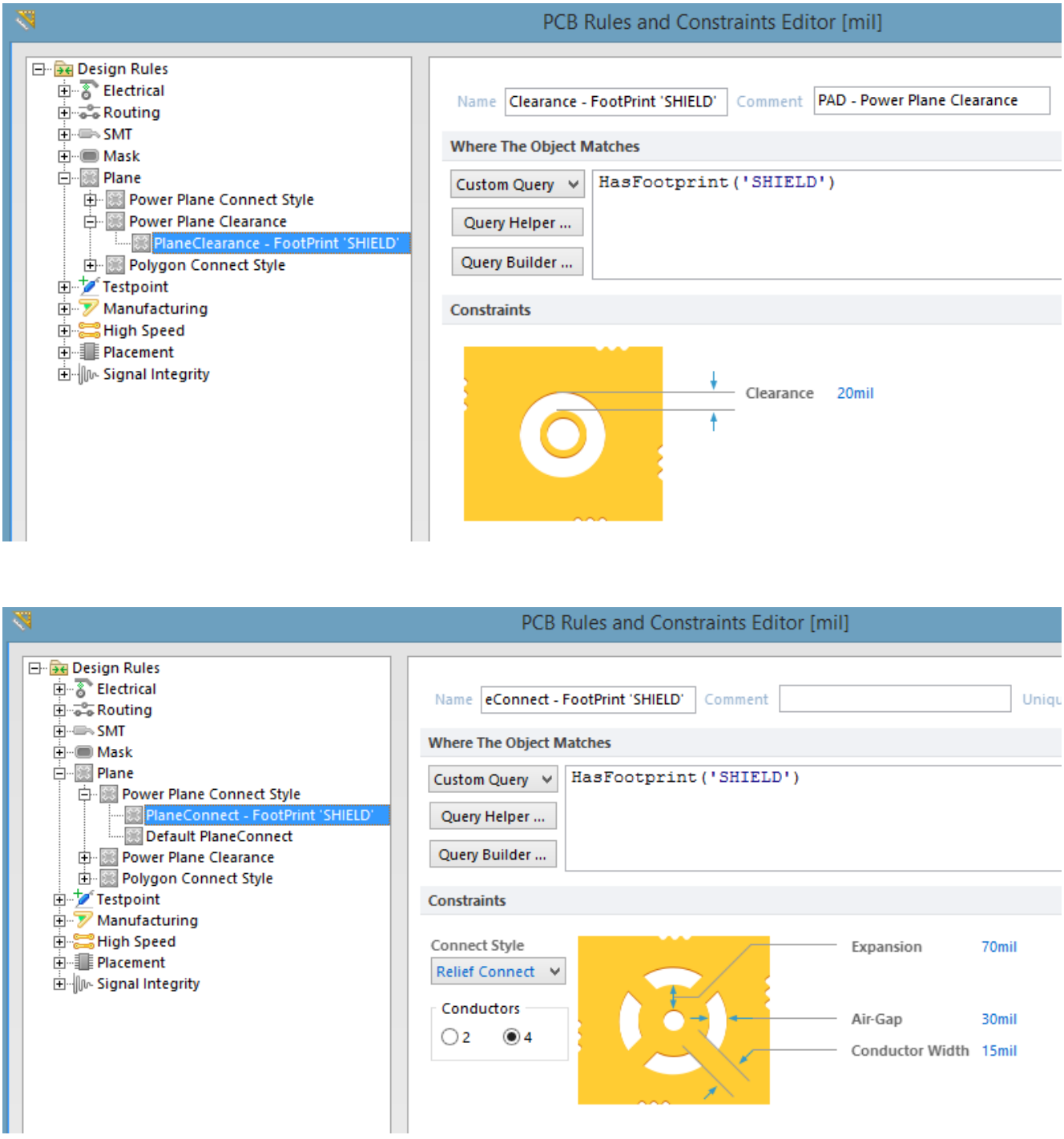
As discussed in the Layer Mapping section of the Import Process, PADS CAM planes are defaulted to map to Altium Designer plane (negative) layers, and split/mixed layers can also map to Altium Designer negative planes as split layers.

If this is the case, then any connectivity and clearance rules are also set in the design rules of Altium Designer. Again, because of the many locations these rules can be set in PADS, they may or may not all get successfully converted (for instance, padstacks using Layer_25 for thermal or clearance values will not translate). Therefore, creating specific plane rules may be necessary. However, if any PADS padstacks have a specific thermal or antipad value set, a corresponding Plane Connect or Plane Clearance rule will get created in Altium Designer automatically.



Configuring pad stack properties in PADS

While a thermal or antipad value can be applied to a specific pin or component in PADS, when this rule is translated it will be targeted to the footprint. Therefore, any component in the design that uses this footprint will be affected.



Configuring design rules for plane thermals and clearances in Atlium Designer

TRANSLATING YOUR COMPONENT LIBRARIES

COMPONENT LIBRARY IMPORTING PROCESS

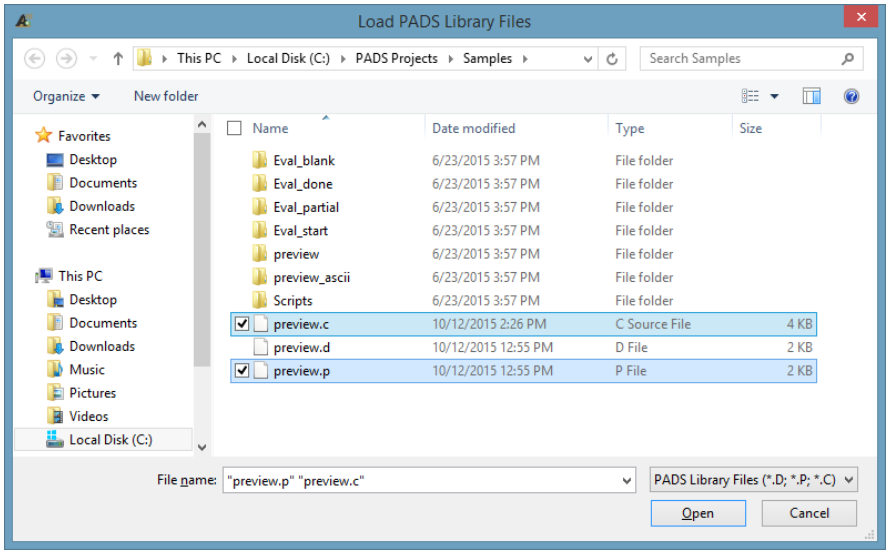
Translating PADS Libraries can be accomplished with the steps below:

1. Select **File » Import Wizard**.
2. Select **Next** on the welcome screen, choose 'PADS ASCII Design and Library Files' and select **Next** to continue.
3. Select **Next** again to skip the Design Import screen.
4. On the Importing PADS Libraries screen, select **Add** to load one or more library files.

Schematic Symbol Libraries

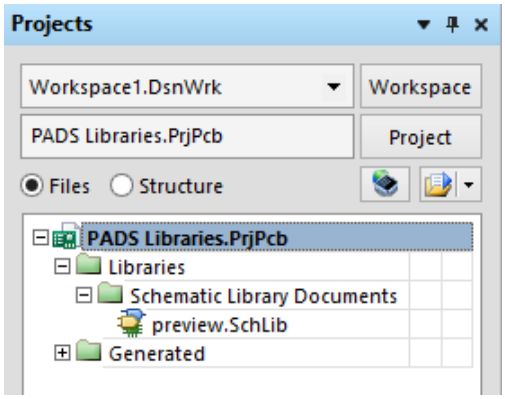
As discussed in the ASCII File creation section, translating schematic symbol libraries requires two files – the '.c' and the '.p' – in order to create the Altium Designer schematic symbol library correctly.

5. In the Load PADS Library Files browser, select both the '.c' and '.p' files of the library to be translated and select **Open**.



Loading PADS library files in the Altium Designer Import Wizard

6. Select **Next** two more times to begin the translation process. When the process is complete, the translated schematic library can then be opened from the Projects panel.

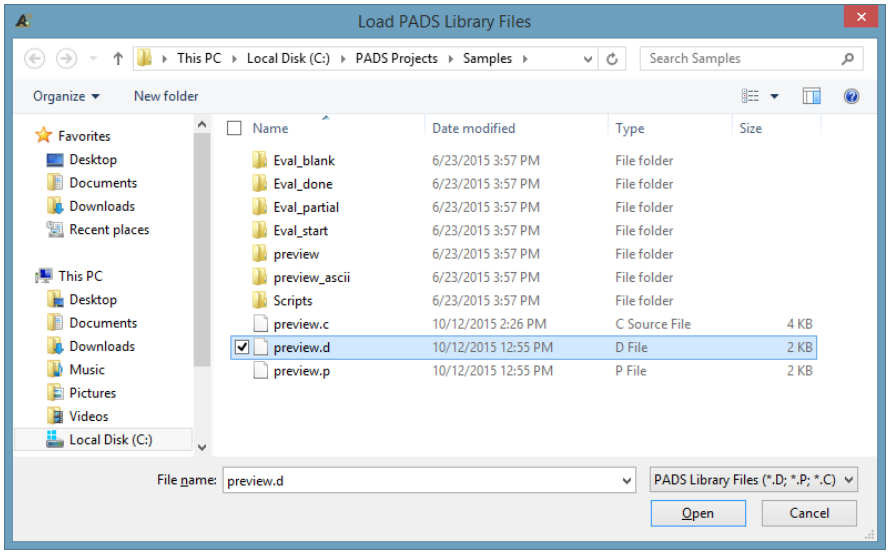


Projects Panel in Altium Designer

PCB Decal/Footprint Libraries

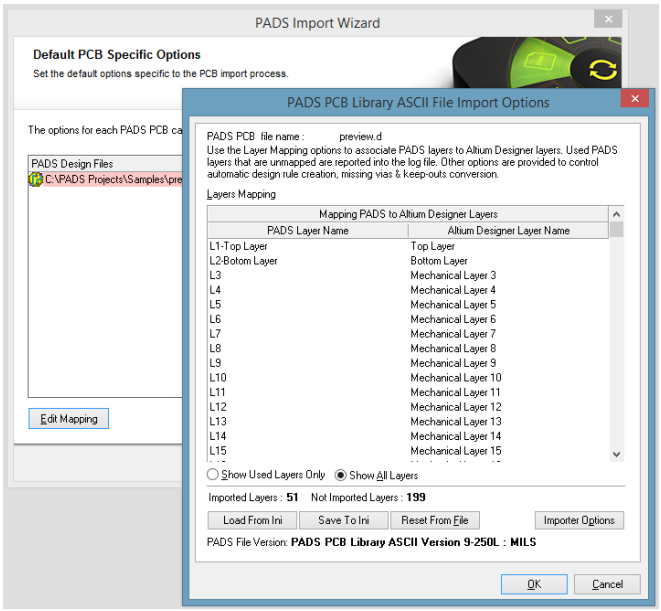
Importing the PADS Decals follows the same process, except that the file to load will have a *'.d'* extension.

7. Select the file(s) to be translated and select **Open**.
8. Select **Next** twice to continue through the wizard.



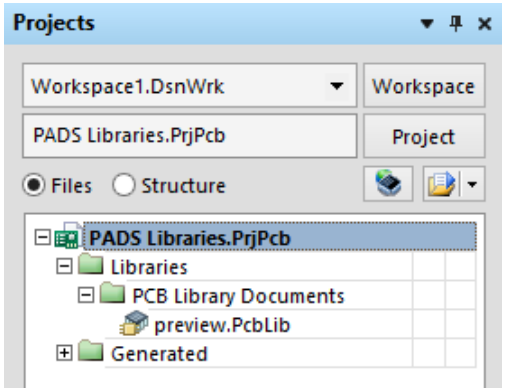
Loading PADS decal and footprint libraries

For a decal file import, there is a Layer Mapping option in the Import Wizard, similar to that of the PCB Design Layer Mapping. Again, attempts are made to map like-layers (silkscreen-to-silkscreen, etc.) As a reminder, it is not required to have all PADS layers mapped to an Altium Designer layer.



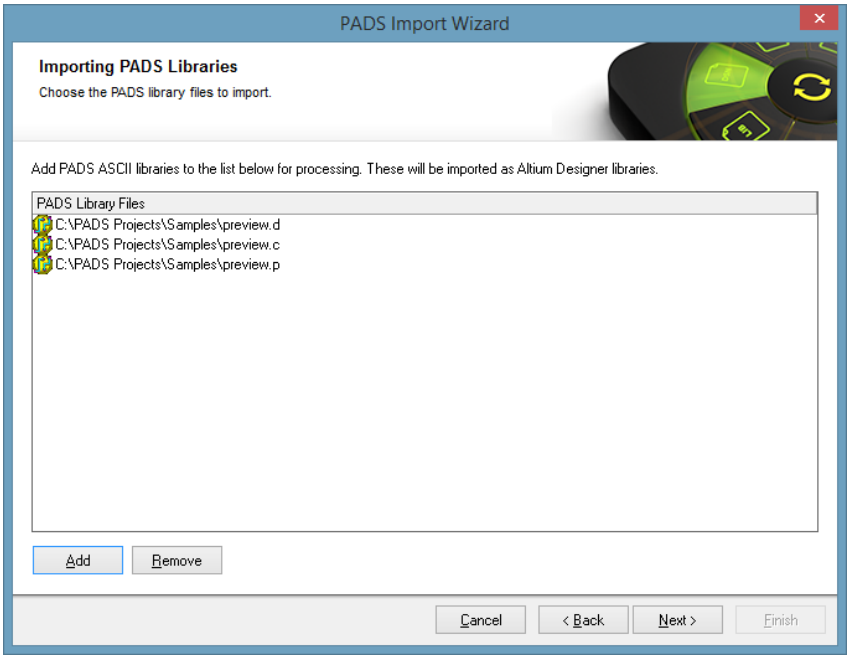
Configuring layer mapping options in the Import Wizard

9. Once the layer has been mapped, select **Next** twice more to begin the translation.
10. After translation, the PCB footprint library can then be opened from the Projects panel.



Project Panel in Altium Designer

TIP: Schematic symbol libraries and PCB decal libraries can be translated during the same import process.



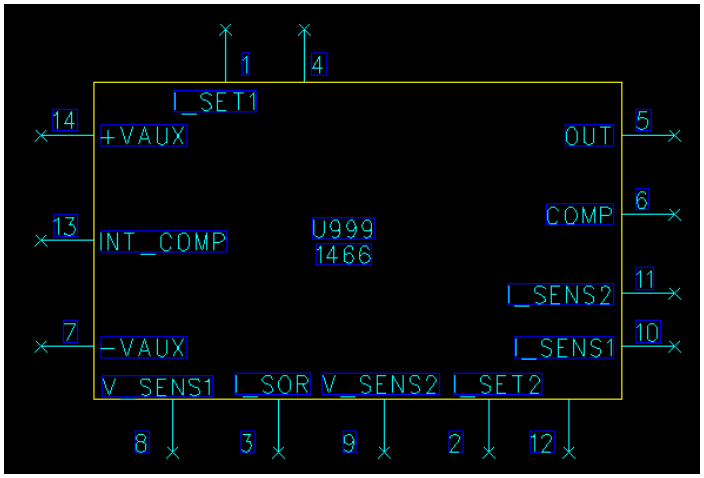
Summary of imported libraries in the Import Wizard

SCHEMATIC SYMBOL LIBRARY CLEANUP

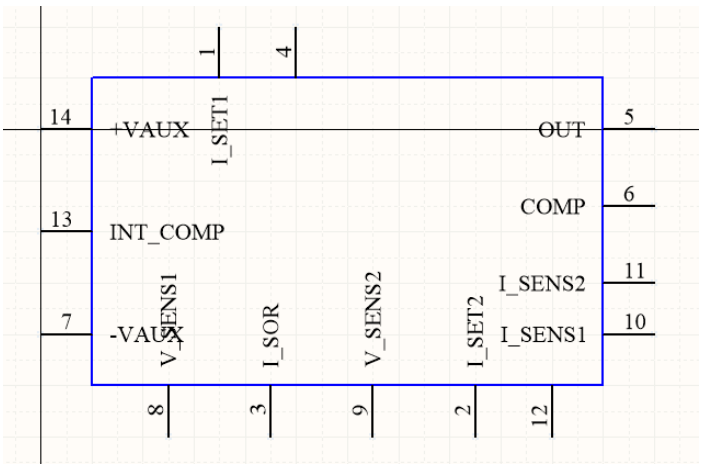
Most aspects of the schematic symbols translate accurately – including symbol graphics, pin names and numbers, parameters, and pointers to decals/footprints. However, some minor symbol library editing may be necessary. Here are some examples:

Text and Pin Name Locations

Differences in the default PADS fonts can cause the overall size and positioning of pin names and numbers not to match up 100%. Also, pin names are reset to their default location and orientation, which is directly in-line with the pin.

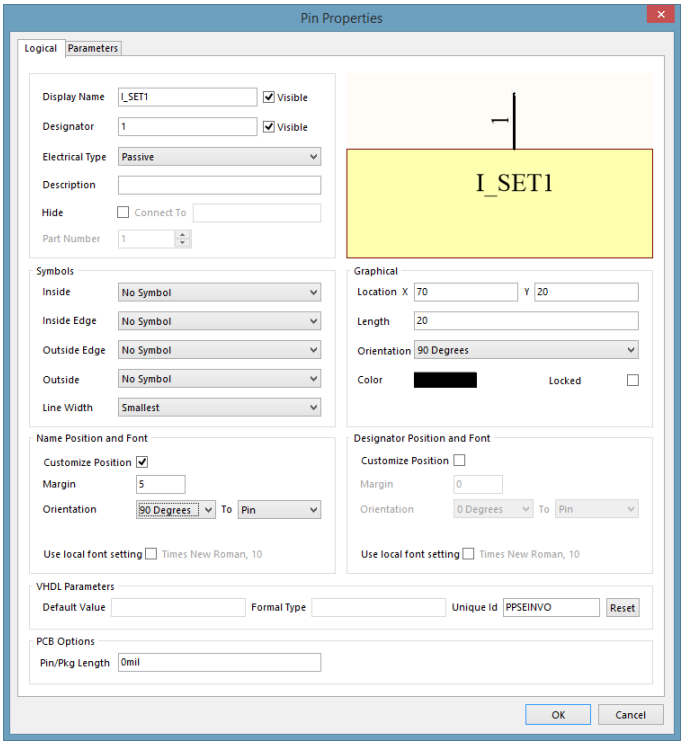


Symbol in PADS



The same symbol in Altium Designer with pin names along the top and bottom rotated back to 0 degree rotations.

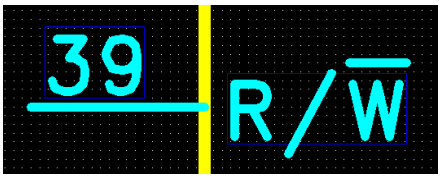
Pin names can be adjusted in Altium Designer using the 'Customize Position' settings in Pin Properties dialog as shown below.



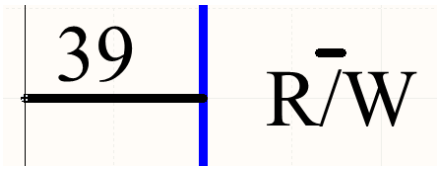
Customizing pin properties in Altium Designer

Inverted and Negated Pins

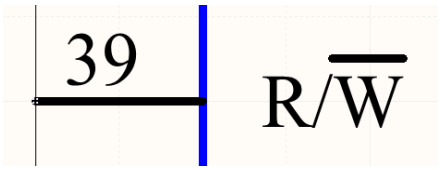
As discussed in the Schematic Cleanup section, inverted signals in Altium Designer are defined differently than in PADS. Pin (signal) names are subject to the same settings and should be modified. See the examples below for differences between PADS and Altium Designer.



Pin example in PADS



Same pin example in Altium Designer



The Pin Name text needs to be changed from "R/\W" to "R/W\" (move the backslash after the W)

FOOTPRINT LIBRARY CLEANUP

Most aspects of the PCB decals translate accurately – including pin numbers and padstacks, silkscreens, copper shapes, etc. However, some minor footprint library editing may be necessary.The areas to investigate are:

Keepouts

As discussed in the Keepouts section of PCB Cleanup, there are a considerable number of differences in the capabilities of keepouts in PADS vs. Altium Designer. As it relates to the footprint library, however, there is really only one situation that will need attention. A PADS keepout can be configured to keep out individual object types. It is common to place via-specific keepouts in footprints (e.g., between pins of a capacitor).

PADS via keepout areas translate to keepout regions in Altium Designer which will keep out all electrical objects. There is no equivalent via-only keepout object in Altium Designer, so this type of keepout should either be removed, or the impact of the changes understood.

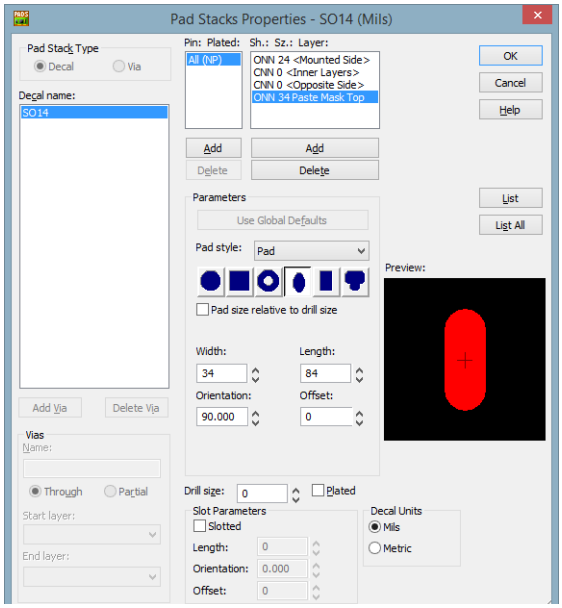
Another common footprint specific keepout is a copper pour keepout. A keepout configured as a pour keepout will also be translated as a complete keepout in Altium Designer. However, polygon pour cutouts can be added to an Altium Designer footprint (**Place » Polygon Pour Cutout**), correcting the situation. After adding the polygon pour cutout, remember to remove the original keepout object.

Solder mask and Paste mask

Altium Designer automatically adds solder and paste masks over/undersize values by a default rule. If those layers were specifically defined in PADS, then the padstack values will be set accordingly in Altium Designer. If no solder mask and/or paste mask layers were defined, then the Altium Designer default settings will be used.

For example, there is a paste mask top layer added to the padstack with a 5 mil oversize (5 mils added in each direction to increase the 24 mil solder mask clearance to 34 mil).

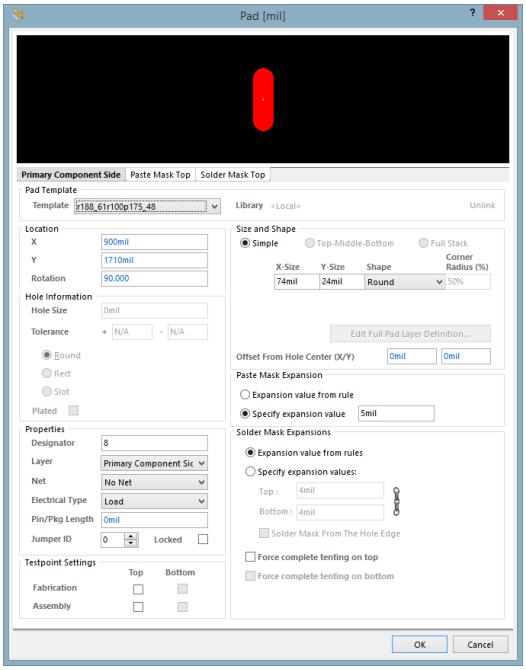
The 5 mil value will then be applied to the "Paste Mask Expansion" value in the Altium Designer pad properties. As there was no solder mask layer added to the padstack in PADS, the default setting of Expansion value from rule is used.



Configuring pad stack properties in Altium Designer

PADS allows the mask expansions to oversize/undersize the width and length independently. So in this example, the pad width was increased from 24 mils to 34 mils, but the pad length of 74 mil could have stayed at 74 mil on the paste mask layer. Because Altium Designer applies the expansion values in all directions (i.e., it "grows" or "shrinks" the total pad size), it is important look for any pads that may have had these non-uniform over or undersize values.

TIP: If there is a difference between the width and length expansion values in PADS, the smaller value will be used when translating into Altium Designer.

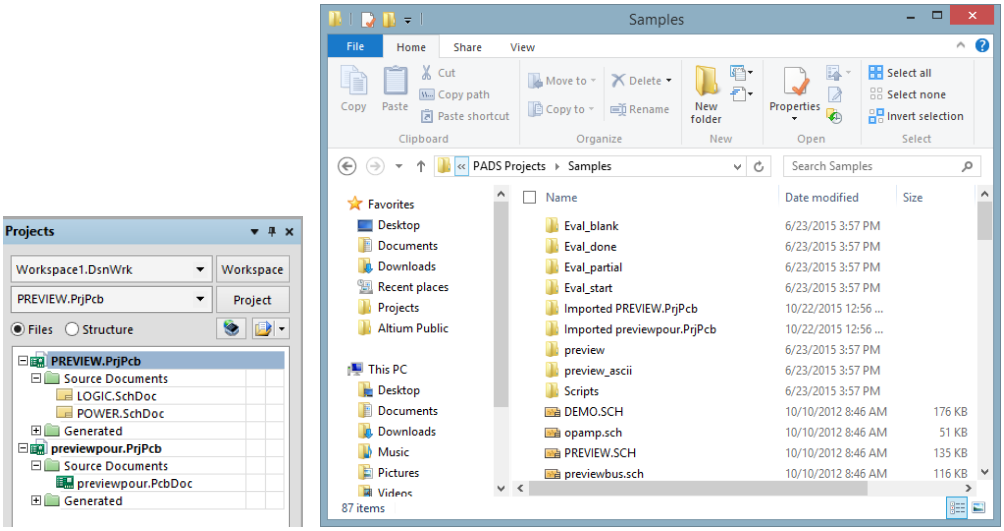


Configuring pad properties in Altium Designer

SYNCHRONIZING YOUR SCHEMATICS AND PCBS

PROJECT MANAGEMENT

Although schematic and PCB designs can be translated during the same Import Wizard session, the translations are run as separate processes. When each design is translated, the resulting files will be placed into separate projects. In this example, the "Preview" schematic and ***"Previewpour"*** PCB design were run through the Import Wizard at the same time, but two separate projects and project folder structures were created.



Working with two separate projects imported into Altium Designer

If it is necessary to fully recreate the project, then some file management will need to be done. It is generally recommended that all project files reside in the same folder. Since there are usually multiple schematic documents and only one PCB document, the simplest thing to do is copy or move the '*.PcbDoc*' file into the project folder where the '*.SchDoc*'(s) reside.

At this point, the imported PCB project is not needed ("previewpour.PrjPcb" in this example) so it can be closed. Right click the project name in the panel ("previewpour. PrjPcb") and click Close Project. "Preview.PrjPcb" is now the working project from this point forward. The '.PcbDoc' file now needs to be added to the project. Go to **Project » Add Existing to Project**, add the '*.PcbDoc*' file and then save the Project.

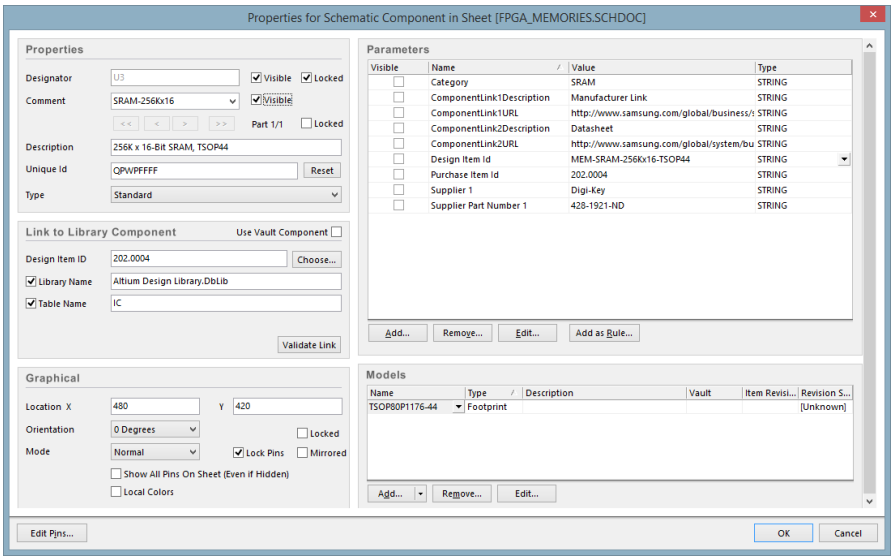
For more information on projects refer to Project Management within TechDocs.

SYNCHRONIZATION

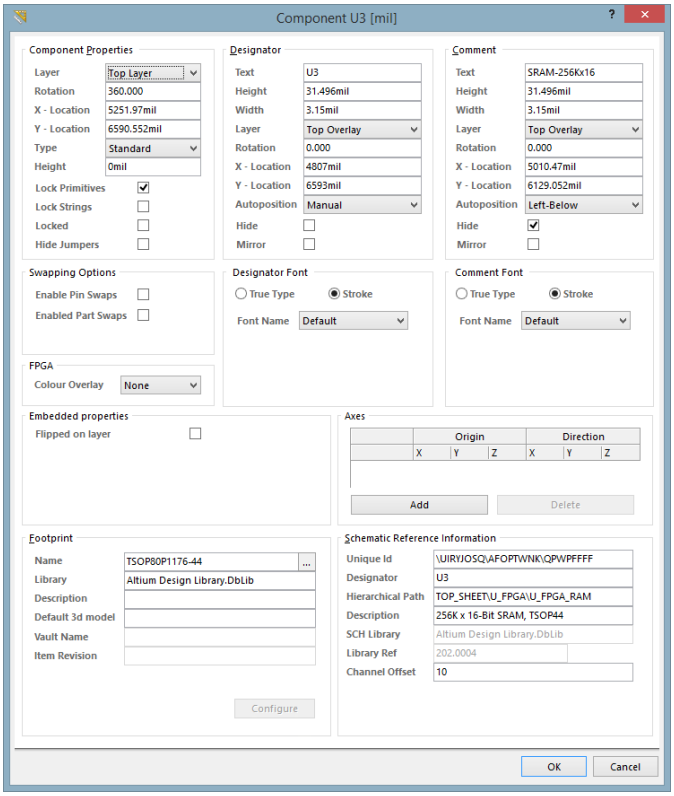
Instead of using Reference Designators to synchronize the schematic and the PCB, Altium Designer uses a Unique Id value. This can be thought of as a unique serial number for each component. When creating a design from scratch in Altium Designer, each component automatically receives a system-generated Unique Id within the schematic editor.

When the design is transferred to the PCB editor, that Unique Id is passed over and resides on the corresponding footprint within the PCB document. In the example below, 'U3' is assigned Unique Id "*QPWPFFFF*" which can be seen in both the schematic and PCB editors.

Note: The extra ID values seen in the footprint ("\UIRYJOSQ\AFOPTWNK\") are due to the hierarchical nature of this particular design.



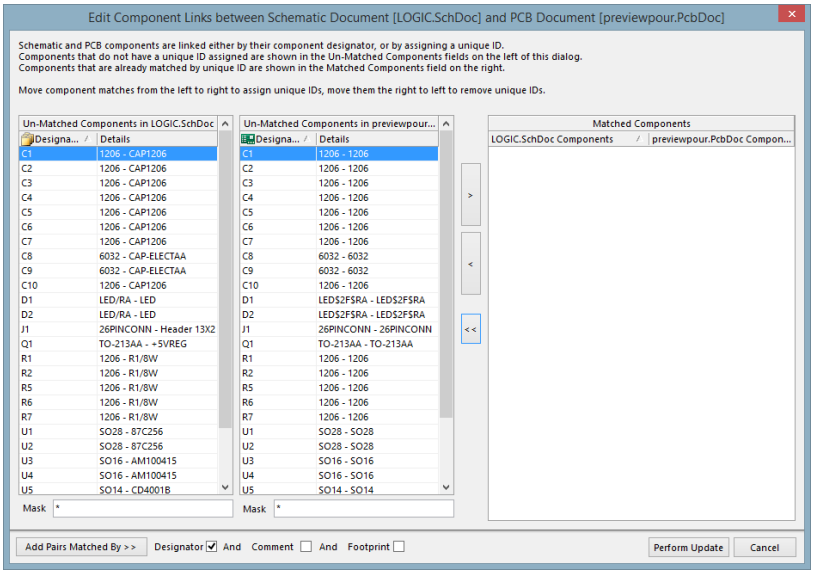
Configuring properties for schematic components in Altium Designer



Configuring component properties in Altium Designer

When the PCB designs are translated from PADS Layout, the Unique Id values are not assigned, because matching to an existing schematic cannot be guaranteed. Fortunately, there is a very simple process to synchronize the Unique ID values from the translated schematic to the translated PCB design. Follow the steps below to accomplish this

1. Open the *.PcbDoc* file, and go to **Project » Component Links**.

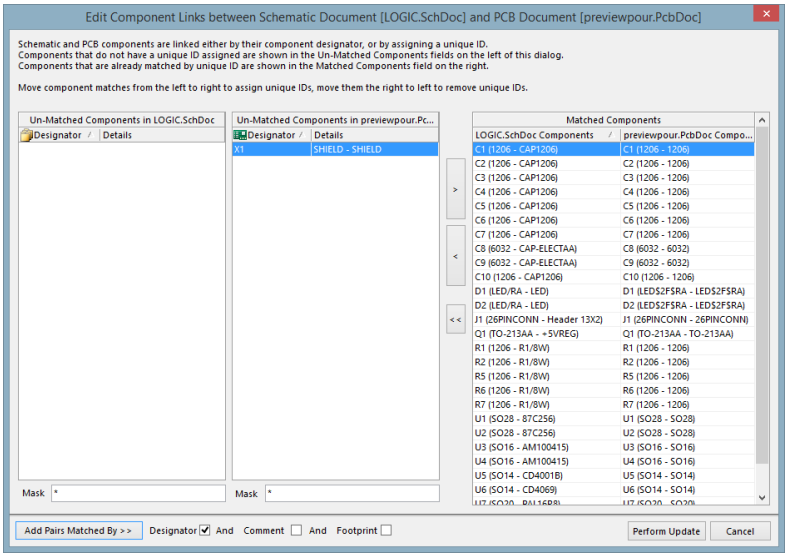


Configuring component links between a schematic and PCB

Any components in the two left-hand panes do not have matching Unique IDs. The goal here is to match a schematic component with a PCB component. This can be done manually by selecting a pair and adding (using the > button) it to the right-hand 'Matched Components' list.

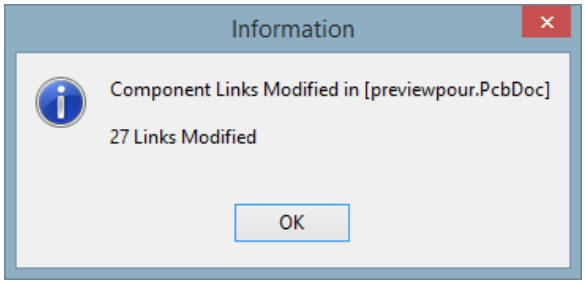
There is also an automated method which will look at any combination of Reference Designator, Comment and Footprint. Since this design was originally done fully in PADS, it is safe to assume that the reference designators are a direct match between schematic and PCB.

2. Ensure the **Designator** checkbox is enabled (disable **Comment** and **Footprint**).
3. Click the **Add Pairs Matched By >>** button. This will automatically pair the schematic and PCB components by their reference designators.



Pairing schematic and PCB components by their reference designators in Altium Designer

4. Select **Perform Update** to sync the Unique Id pairs.
5. Click **OK**.

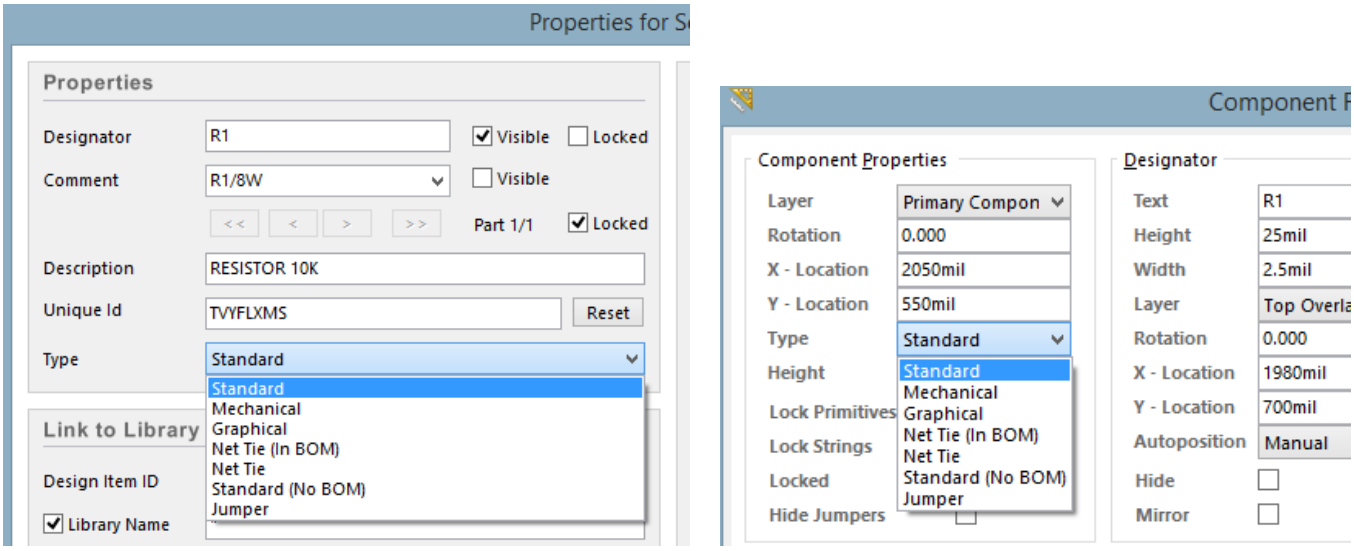


Component link confirmation

This will now enable functions like cross-probing and Engineering Change Orders (ECOs) to operate much more accurately.

It is worth noting that, as in the example above, there may not be a complete 1-to-1 match in the reference designator list. This may be due to mechanical type components added to the board but not the schematic, as in the "Shield" component above. Mounting holes added as components are another common mismatch. The reverse situation may also be true where a component was added to the schematic as to be included in the BOM, but has no physical representation in the PCB, like a heat sink.

Whereas PADS handles these situations using the ECO Registered property, Altium Designer has several different component property options to define the ECO behavior. Component properties in both the schematic and PCB editors include a list of available component types as shown below.



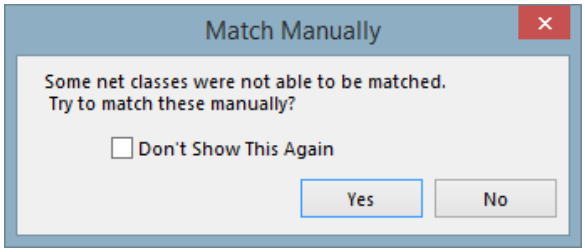
Configuring property options for ECOs in Altium Designer

You're able to read more about Altium Designer component types in A Look at Creating Library Components article.

Setting the "Shield" (X1) component to Mechanical will remove it from the Component Links dialog. More importantly, it will also make the ECO process ignore X1 as a missing component. Otherwise, X1 would be removed during an ECO as it has no schematic counterpart.

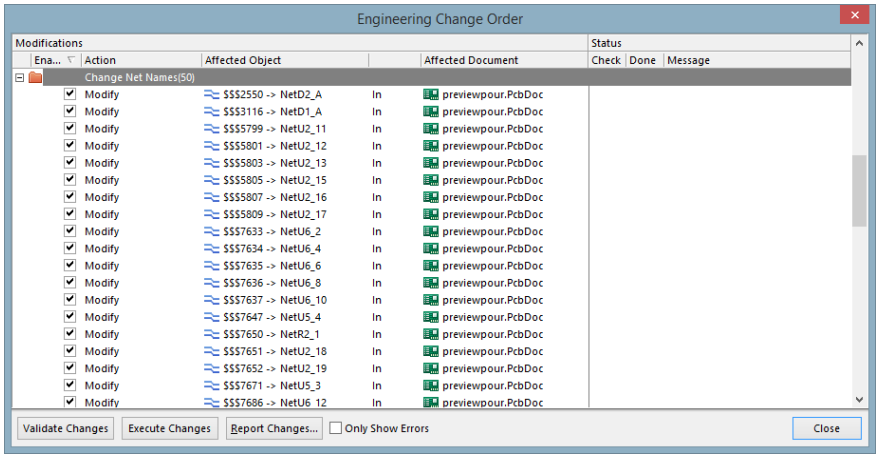
Engineering Change Orders

Performing an ECO at this point should point out any remaining inconsistencies between the schematic and PCB. From the PCB, go to **Design » Import Changes from <project name>**. A message window (or two) may appear asking to manually match net names and/or classes. The best thing to do initially is select **No** here and go through the rest of the ECO process to rename any nets or make any other changes.



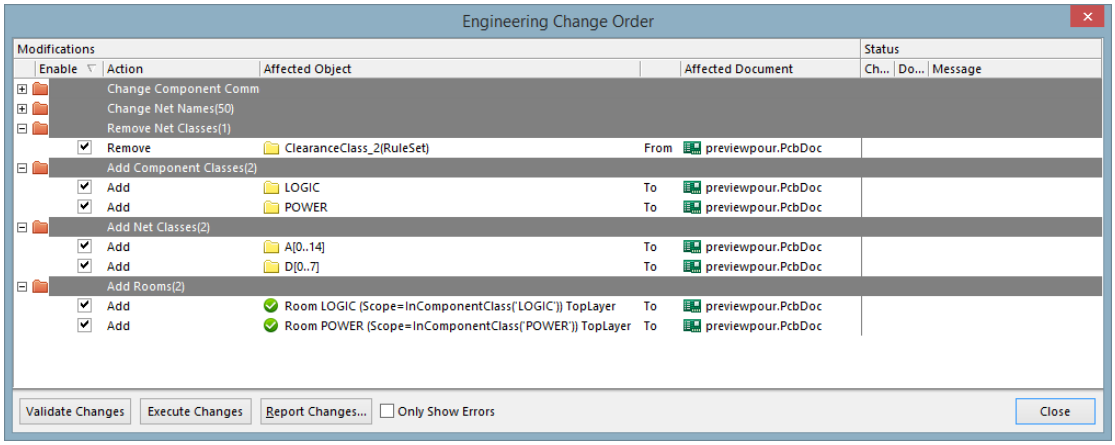
Manually matching net names/classes confirmation

While there may be many changes required by the ECO process, one of the more important tasks is to rename the system-assigned net names. As discussed in the Schematic Import Process section, PADS Logic and Altium Designer create systemassigned net names differently. It is generally recommended to allow the ECO process to rename the PADS names to the Altium Designer names as shown below.



System assigned net names in Altium Designer

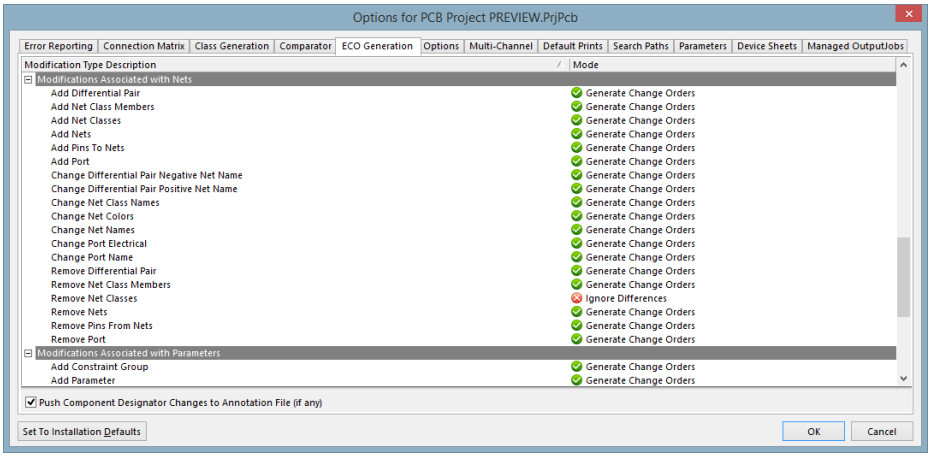
Some other changes that may be requested by the ECO process can be controlled via the **Project » Project Options**. Altium Designer will, by default, attempt to create, remove, and/or synchronize net classes, component classes, rooms, etc.



Configuring project options for an ECO in Altium Designer

It is up to the user whether to accept these changes or not. The checkboxes in the ECO dialog allow the user to temporarily disable any particular change. Permanent changes to the types of modifications that are made during an ECO are controlled in the **Project » Project Options** menu, and then setting up the options in the **ECO Generation** tab.

One important option that usually needs changing is **Remove Net Classes**. Altium Designer attempts to synchronize the net classes created in the schematic and those created in the PCB. If there were any net classes created during the design rule translation, and/or if net classes were defined in PADS Layout but not in PADS Logic, then the ECO process will, by default, attempt to remove them in order to have the PCB exactly match the schematic.

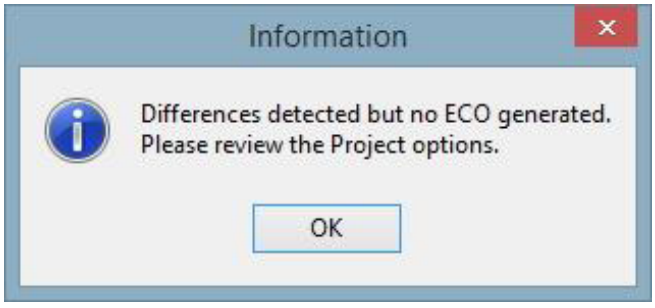


Configuring project modification options for ECOs in Altium Designer

Setting the **Remove Net Classes** option to 'Ignore Differences' prevents any net classes that exist only in the PCB file from getting removed.

There are many other situations which will cause the ECO process to show differences between the schematic and PCB. They cannot all be discussed here, but the user should be able to determine the sources of the differences by using the concepts provided here. For more information go to Finding Differences and Synchronizing Designs within TechDocs.

Ultimately, the goal is to receive a message after performing an update that says that no ECO will be generated, or that no differences are found (this will depend on how the Project Options are set).



No differences dialog

YOUR NEXT STEPS IN ALTIUM DESIGNER

With all of your design files successfully translated from PADS, it's now time to dive deeper into the intricacies of the Unified Design Environment in Altium Designer. We've included several links below to our documentation, video tutorials, and additional training resources that will help you make the most of your experience in Altium Designer.

SUPPORT DOCUMENTATION

- From Idea to Manufacturer – Explore a complete set of tutorials for creating your first schematic and board layout in Altium Designer.
- Exploring Altium Designer – Get a complete overview of the Unified Design Environment in Altium Designer.
- More About Components & Libraries – Learn how to easily manage your component libraries in your Altium Designer workspace.

That's just a small sampling of all the documentation available for Altium Designer. Explore more at Altium Documentation.

VIDEO LIBRARY

Our complete suite of videos includes several tutorials, feature overviews, and more to help introduce you to the Altium Designer environment. View all the available videos on the Altiumlive Video Library.

LIVE TRAINING EVENTS

Prefer a more hands-on approach to your learning? Register for one of our live events including webinars, training courses, or seminars. View all the events on the Altium Events page.

NEED ADDITIONAL HELP?

Our support team is always here to assist you with any questions you might have. You can contact us directly through the Contact Us page.

© 2017 Altium LLC. PADS® is a registered trademark of Mentor Graphics Corp.